High Frequency Link Current Estimation Based Control of Solid State Transformer

A thesis submitted

in partial fulfillment for the award of the degree of

Doctor of Philosophy

by

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April 2025

Certificate

This is to certify that the thesis titled ***High Frequency Link Current Estimation Based Control of Solid State Transformer*** submitted by **Gourahari Nayak**, to the Indian Institute of Space Science and Technology, Thiruvananthapuram, in partial fulfillment for the award of the degree of **Doctor of Philosophy** is a bona fide record of the original work carried out by him/her under my supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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Declaration

I declare that this thesis titled ***High Frequency Link Current Estimation Based Control of Solid State Transformer*** submitted in partial fulfillment for the award of the degree of **Doctor of Philosophy** is a record of the original work carried out by me under the supervision of **Dr. Anindya Dasgupta**, and has not formed the basis for the award of any degree, diploma, associateship, fellowship, or other titles in this or any other Institution or University of higher learning. In keeping with the ethical practice in reporting scientific information, due acknowledgments have been made wherever the findings of others have been cited.

Place: Thiruvananthapuram
Date: April 2025

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This thesis is dedicated to my Parents and my Family . . .

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Gourahari Nayak

Abstract

The pressing need to address climate change demands substantial transformations within the power and transportation sectors, centering on the adoption of sustainable energy sources. A crucial aspect of this transition is the decarbonization of these sectors. Traditional line frequency transformers (LFTs) are inadequate for handling the intermittent, dynamic and bidirectional power flows introduced by renewable energy sources and electric vehicles (EVs). Solid State Transformer (SST) is emerging as a promising solution owing to their sophisticated control functionalities, compact form factor and adeptness to manage these new demands in modern power distribution systems. At the heart of the SST lies the Dual Active Bridge (DAB) converter, acting as the central power processing unit orchestrating the power flow. The critical component within the entire system is the high-frequency link (HF-link) transformer of DAB. Therefore, an effective control strategy must acquire HF-link current information to provide overcurrent protection and safeguard this transformer against saturation, ensuring system stability under varying conditions. Many reported control techniques rely on measuring HF-link current, requiring a high-bandwidth (HBW) current sensor, high sampling frequency ADC and additional signal processing circuitry, hindering overall cost-effectiveness and compact design. Many other reported current control methods use a reduced-order dynamic model that excludes HF-link current as a system state variable, failing to provide any information about the critical high frequency transformer.

This thesis attempts to contribute to a broader endeavour by developing a HBW current sensorless control strategy based on state estimation. Its goal is to control the power flow and provide pre-emptive overcurrent saturation protection by gathering the HF-link current information through estimation, instead of directly measuring it.

Additionally, this thesis addresses the key challenges associated with the modular configuration of SST by extending the developed control strategy for a single DAB module to modular SST configurations. Modularity allows for scalability, simplified maintenance, design flexibility, system reconfiguration and enhanced reliability through redundancy. This thesis considers two types of modular configurations: input-series-output-parallel (ISOP) and input-parallel-output-parallel (IPOP). It is inevitable to have parameter mismatches across the cells of modular SST, especially unequal leakage inductances of HF-link transformers, which invariably lead to unbalanced DC-link voltages and unequal power distribution. While many reported control methods focus on power balance control strategies, this thesis attempts to establish the need for flexible power sharing control capable of facilitating equal power sharing, controlled unequal power sharing and zero power sharing (plug-in/plug-out operation) depending on normal or contingency situation.

To meet the set of objectives, efforts are directed towards developing HBW current sensorless control method, relying on the estimation of the fundamental component of HF-link current, to achieve flexible power sharing control in both modular ISOP and IPOP SSTs. Additionally, the process of parameter identification for the HF-link inductance is explored to effectively tackle parametric variations. In the IPOP configuration, it is attempted to achieve unity power factor (UPF) operation of multiple parallel modules connected to grid, using a single low bandwidth current sensor.

The developed methods are validated through simulations and extensive experimental results. The proposed solutions in this thesis have the potential to enhance reliability, achieve seamless power flow and reduce cost of the SST system.

Contents

List of Figures

List of Tables

Abbreviations

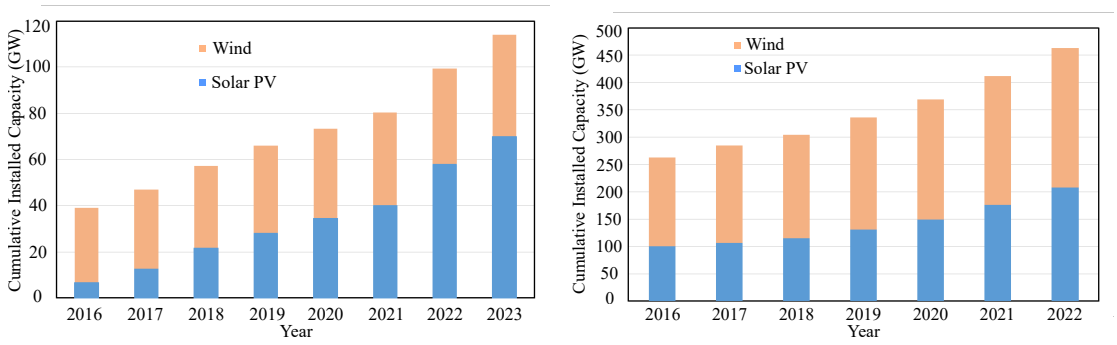
SST	Solid State Transformer
HFAC-L	High Frequency AC Link
CMFEC	Cascaded Multilevel Front End Converter
DAB	Dual Active Bridge
HF-Link	High Frequency Link
ISOP	Input Series Output Parallel
MVAC	Medium Voltage AC
MVDC	Medium Voltage DC
LVDC	Low Voltage DC
HBW	High Bandwidth
GA	Generalised Average
SPS	Single Phase Shift
THD	Total Harmonic Distortion
IPOP	Input Parallel Output Parallel
IPFEC	Input Parallel Front End Converter
OPDAB	Output Parallel Dual Active Bridge

Chapter 1

Introduction

1.1 Background

For the last couple of decades, combating global warming has been the guiding philosophy behind rethinking and reforming the power sector. The 2015 Paris Agreement sets a long-term goal, aiming to limit the rise in global mean temperature by 1.5°C [1], which would significantly mitigate the impacts of climate change. The agreement stresses on stringent emission reductions with the ultimate aim of achieving net-zero emission globally by the middle of this century. Many countries are making significant strides in this direction by adopting more and more green energy sources also known as renewable energy resources



(a) Installed capacity in India. **(b)** Installed capacity in EU.

Figure 1.1: Renewable energy (solar and wind) installed capacity.

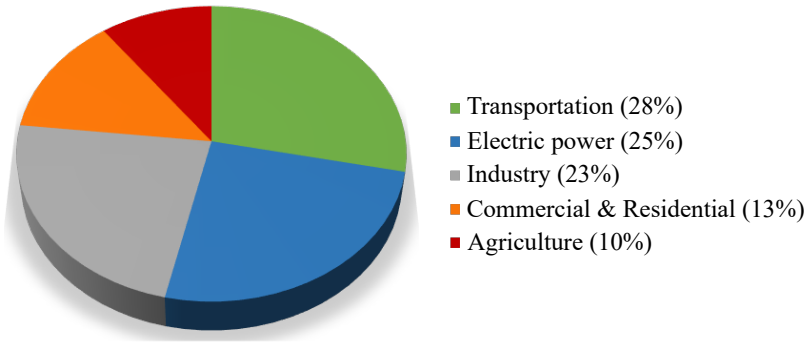
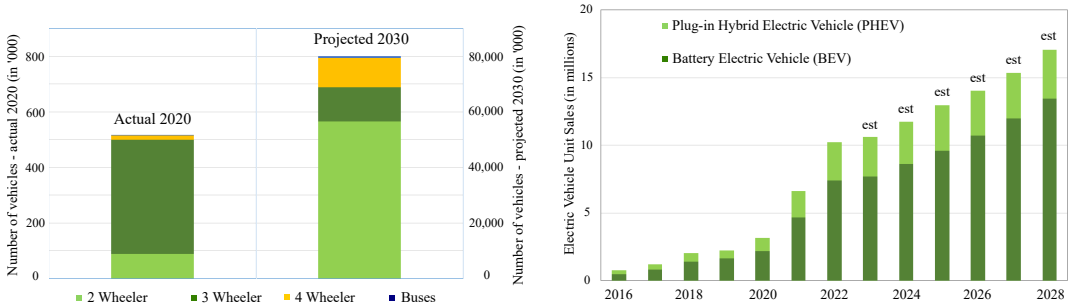


Figure 1.2: Emission from various sectors.

(RER) by implementing various policies and regulations. Fig. 1.1 depicts the increment in total solar and wind energy installed capacity of India and EU [2, 3, 4].

The green house gas emission from power generation and transportation sector combined is nearly 53% as shown in Fig. 1.2 [5]. The decarbonization of transport sector is expected to be a pivotal factor in accomplishing these objectives. New policies by the governments can serve as catalysts for the evolution of green transportation by mandating the widespread adoption of electric vehicles (EV). The actual and projected number of EV unit sales of this decade are highlighted in Fig. 1.3 [6, 7]. Netherlands, France, India are few examples who have announced their plans to work towards zero-emission vehicles by culminating sales of internal combustion engine vehicles by 2025, 2030 and 2040 respectively. Hence the EV market is poised to go through a substantial change soon.



(a) India - Number of EV unit sales. **(b)** Global EV sales.

Figure 1.3: Projected electric vehicle (EV) sale for this decade.

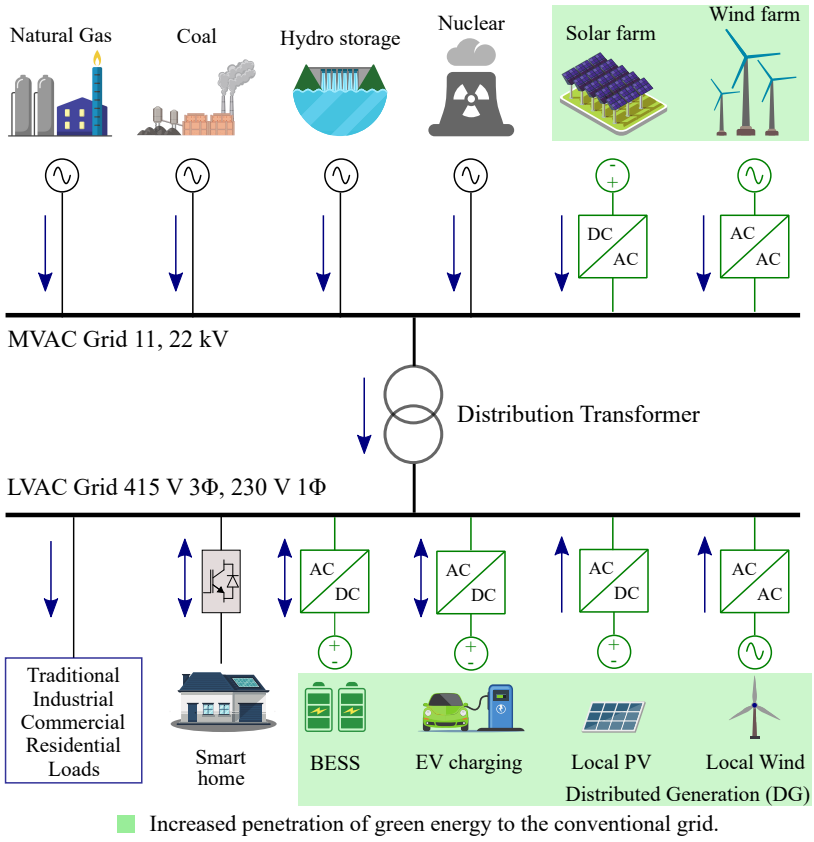


Figure 1.4: Power distribution system with increased penetration of RERs, BESS, EVs.

The adoption of distributed energy resources (DERs), EVs and BESS in the active distribution networks is increasing rapidly. These are expected to increase further for achieving the net-zero emission goal. A block diagram showing the increased penetration of green energy sources and loads in the modern day distribution network is shown in Fig. 1.4. The increasing integration of DERs into the conventional grid creates new challenges due to their intermittent nature. Similarly, the incorporation of EV charging stations (EVCS) into the conventional grid can give rise to various challenges, primarily due to grid-to-vehicle (G2V) and vehicle-to-grid (V2G) bidirectional charging and discharging functionalities of EVs. Key challenges are power quality issues, harmonic pollution and fluctuation in point of common coupling (PCC) voltage. To meet these emerging requirements on the distribution network, a component that needs significant renovation is the distribution transformer.

Distribution transformer is a crucial component in the distribution system. Its main objective of is to lower the high voltage to a safe level by providing galvanic isolation that can be safely utilized by residential and commercial end-users such as homes, industries and other organizations. Isolation serves to safeguard human users, protect the low voltage circuitry from higher voltages and enhance the circuit's immunity to unwanted noise.

In India, the standard voltage rating of distribution transformers is typically 11 kV or 33 kV medium voltage AC (MVAC) / 415V (3-phase) and 240V (1-phase) low voltage AC (LVAC). The nominal line frequency is 50 Hz. Henceforth, throughout this thesis the distribution transformer will be referred to as the line frequency transformer (LFT). The LFTs can be 1-phase or 3-phase. 1-phase transformer caters to residential and small commercial properties. Meanwhile, 3-phase transformers are used for bigger establishments like factories and commercial buildings. This technology has survived for more than 100 years since its inception because of its superior reliability and exceptional efficiency. However, the LFT is a passive component which is not suitable for rapidly changing load requirements with its on-load tap changer (OLTC) mechanism. These conventional transformers are also bulky and often cooled with oil having potential risk on environment. They also lack control features such as tight voltage regulation, power factor correction, fault current limitation, reactive power compensation and integration of distributed renewable energy resources. These challenges can be addressed by replacing the LFT with a smart energy router equipped with intelligent capabilities to effectively manage and regulate the flow of power. Solid state transformer (SST) is the best candidate which has the capability to overcome these limitations.

1.2 The Solid State Transformer

The fundamental aim of a SST is to achieve voltage transformation using high-frequency isolation, which can result in reduced volume and weight compared to LFT. Solid state

transformers are also commonly known as power electronic transformer (PET), power electronic traction transformer (PETT) and smart transformer depending on its application [8, 9, 10, 11, 12, 13]. A SST based future grid system is depicted in Fig. 1.5. It produces an additional low voltage DC (LVDC) bus to which the DERs, EV charging stations and BESS can be directly integrated.

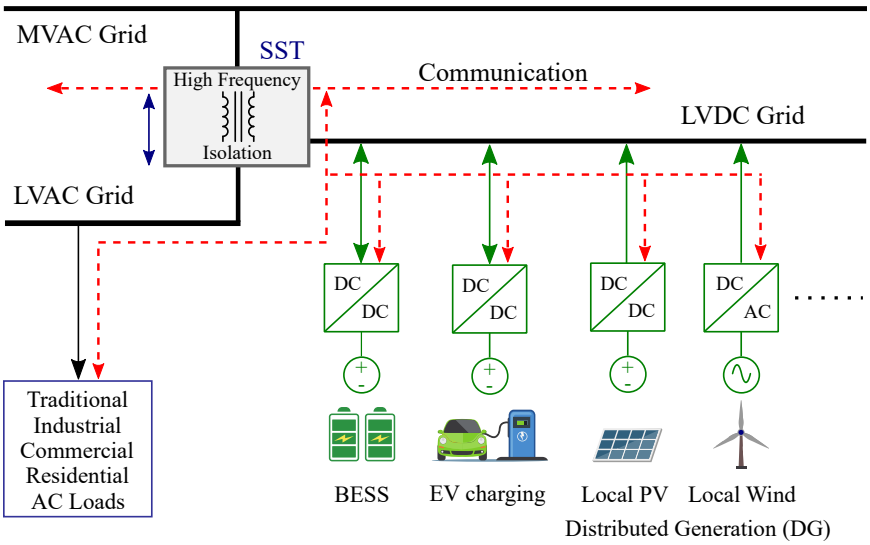


Figure 1.5: Envisioned future distribution grid with SST.

1.2.1 Comparison of SST with LFT

The conventional LFT exhibits several strengths over the SST, including higher efficiency, better reliability, cost-effectiveness and higher overloading capacity [14]. Despite the aforementioned advantages, the conventional transformer experiences certain drawbacks. In LFT, the voltage transformation ratio is adjusted with OLTC. Over its lifetime, the contacts of OLTC can undergo wear and tear due to the thermal and mechanical stresses. The load voltage regulation is poor due to the sluggish response time of these mechanical devices. In SST, the voltage and frequency are controlled by power electronic converters whose response time is much faster. Due to this fast response, it can limit fault current in a controllable manner by isolating the faults quickly. High switching frequency operation is also

Table 1.1: Comparison of SST with LFT.

Parameter	Line frequency transformer	Solid state transformer
Voltage ratio	Adjustable by OLTC	Controllable
Frequency ratio	Fixed	Controllable
Power factor correction	No	Yes
Unwanted harmonic suppression	No	Yes
Voltage regulation	Poor	Tight
Fault current limitation	No	Yes
Swell and sag suppression	No	Yes
Smart energy routing	No	Yes
DER and BESS integration	No	Yes
Reliability	High	Low
Efficiency	High	Low
Cost	Low	High
Weight	High	Low
Volume	High	Low

the main reason for achieving improved power density of SST compared to LFT [15].

Unlike SST, the LFT requires installation of additional shunt active filters, STATCOM, UPQC connected at the point of common coupling (PCC) for power factor correction, harmonic current filtering and improving power quality [16]. The strengths and weaknesses of SST are summarized in Table. 1.1. Given the advantages of SST over LFT, it can emerge as a more viable solution for achieving more compact and better integrated microgrid system.

Microgrid based on SST facilitates controlled bidirectional power flow between main grid-microgrid, microgrid-microgrid (inter-microgrid) and rest of the distribution networks because of the possibility of seamless reverse power flow. Hence SST can work as a smart grid enabler [17]. It also supports information exchange between each element of the distri-

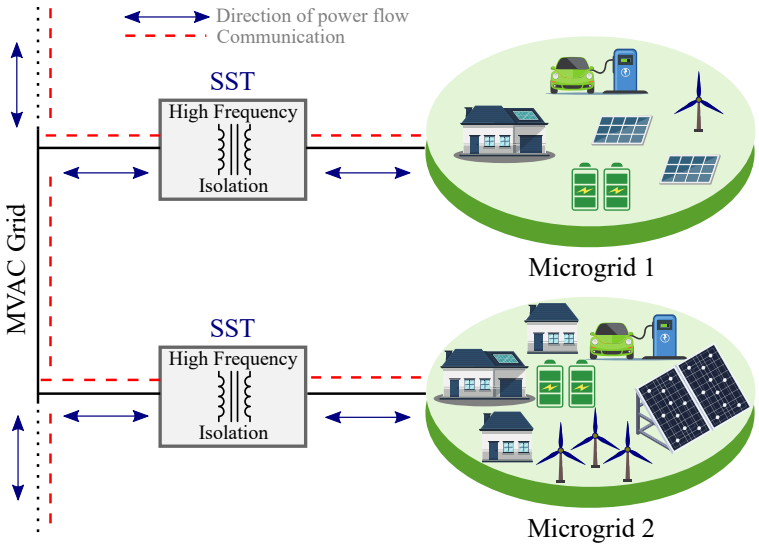


Figure 1.6: Power flow between main grid-microgrid and microgrid-microgrid.

bution system by communication lines. This is presented in Fig. 1.6. The interphase power transfer is also possible in SST due to the availability of a common LVDC bus. However, it is important to note that not all categories of SSTs are suitable for microgrid applications, especially when it comes to meet the requirement of providing all the essential ancillary services.

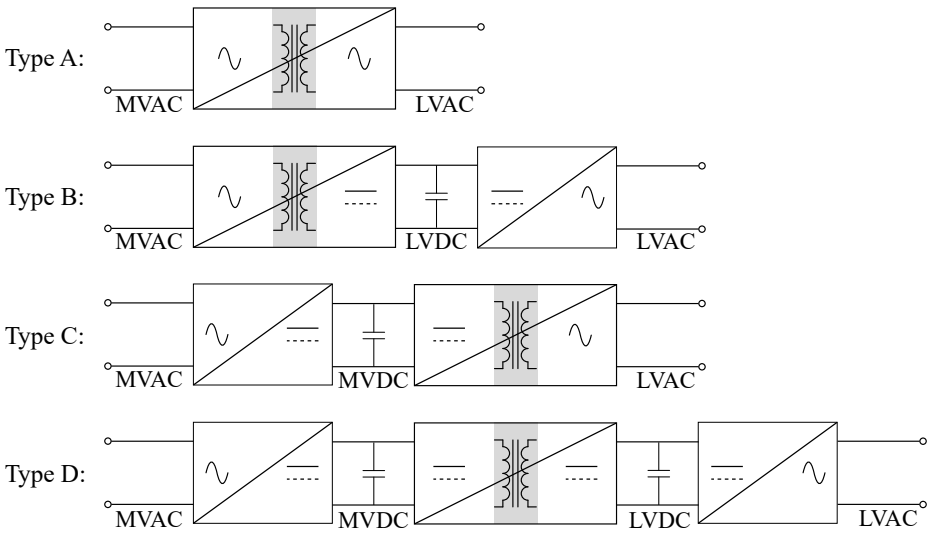


Figure 1.7: Types of SST topology based on power conversion stages.

1.2.2 SST Topological Configurations

There are several variants of SST topology. They are broadly categorized into Type A, Type B, Type C and Type D as shown in Fig. 1.7 [16, 18]. The Type A SST topology is a single-stage SST topology which involves direct MVAC-LVAC power conversion with high frequency link (HF-link) isolation. Type A SST offers low cost, high efficiency, and light weight solution due to usage of less components and simple configuration. The Type B and Type C SST are two-stage topologies. The two power conversion stage for Type B SST are MVAC- LVDC and LVDC-LVAC. Similarly that for Type C SST are MVAC-MVDC and MVDC-LVAC. The Type D SST topology is a three stage SST topology which consists of three power conversion stages: MVAC-MVDC, MVDC-LVDC and LVDC-LVAC. Among the above four types only Type B and Type D SST topologies allows integration of DERs, EV charging stations and BESS due to the availability of the LVDC bus. Hence, only Type B and Type D SST are suitable for smart grid application. The Type B configuration may not be well-suited for high voltage operation due to the challenges in ensuring zero-voltage switching (ZVS) over a very wide MVAC voltage range. In some cases the circuit configuration of two-stage SST and three-stage SST are same. The only difference being in two-stage SST, the MVDC link electrolytic capacitor is replaced by a small AC capacitor to reduce the capacitor size. Hence, the second harmonic ripple power in a 1-phase system gets transmitted from the MVDC side to the LVDC side. For a 1-phase system application, a large electrolytic capacitor is still required at the LVDC bus to suppress this transmitted second harmonic component from MVDC side. For the 3-phase application, as all the output sides of 3-phases are integrated to a common LVDC bus, the total second harmonic ripple power will add up to zero due to the phase differences in 3-phases. However, due to the absence of intermediate MVDC link in Type B two-stage SST, there exists a direct coupling between MVAC and LVDC which can cause the propagation of disturbances from one side to the other. Due to these reasons, the Type D configuration is commonly favoured

because it includes two DC-links, which offer high flexibility and versatility for a wide range of applications. The intermediate MVDC link capacitor prevents the disturbance to propagate from MVAC to LVDC by acting as an stiff energy buffer. A consequence of this is a weak line-load dynamic coupling which facilitates good disturbance rejection capability. It is also observed that the three-stage SST gives superior voltage regulation, fault current limitation, protection, and power factor performance than one or two stage SST [19]. Hence, Type D SST is one of the most preferred choice for many academic as well as industrial applications such as: ABB, GE, EPRI, UNIFLEX and FREEDM system centre [20, 21, 22, 23]. Due to the above mentioned reasons, in this thesis the Type D SST topology is considered.

1.2.3 Modular Topologies

The Type D SST topology can be further categorized into two types: non-modular and modular Type D SST. The non-modular architecture utilizes high-voltage wide-bandgap semiconductor devices for high blocking voltage and high power requirements [24, 25]. Due to the single cell structure the number of switches, DC-link capacitors, HF-link magnetics, gate drivers and sensors required is lower compared to modular structure. However, it lacks scalability which may hamper its suitability for microgrid applications. Additionally, these high-voltage wide-bandgap semiconductor switches have limited commercial availability. Modular SST architecture have several advantages over non-modular structure. Modularity improves reliability due to presence of additional redundancy. Modularity enables reduction in manufacturing costs by leveraging standardized, commercially available low-voltage semiconductor devices. It reduces the electromagnetic interference emission by reducing the dv/dt transition. Through the utilization of modular multilevel converters in a modular SST, it becomes possible to synthesize multilevel waveforms, which in turn, helps minimizing the size of the required filter elements. Additionally, it facilitates

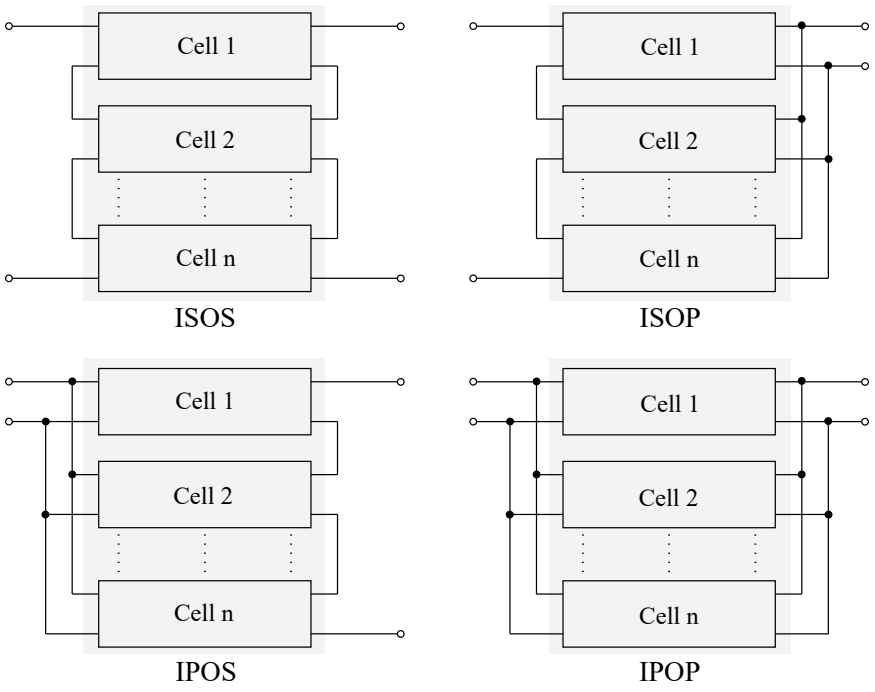


Figure 1.8: Four types of series-parallel connected modular power conversion systems.

easy scalability by providing flexibility to increase power and voltage levels as needed. Modularity also simplifies transportation and installation in challenging locations such as off-shore transmission applications. Hence, considering the reasons mentioned above, the modular Type D SST topology has been chosen for investigation in this thesis to explore its control strategy.

Fig. 1.8 shows four types of modular power conversion systems, these are, ISOS (input-series-output-series), ISOP (input-series-output-parallel), IPOS (input-parallel-output-series) and IPOP (input-parallel-output-parallel) [26, 27]. ISOS configuration is used for application requiring high input voltage and high output voltage. ISOP modular structure is suitable for SST in distribution system application. Many converters can be connected in series at the input MVAC side for high input voltage blocking and in parallel at the output LVDC side for high load current rating. ISOP configuration is also suitable for traction onboard application. IPOS configuration is used for high input current and high output voltage application. Similarly, IPOP configuration is well suited for the high input current and large

output current application. In this thesis the development of control strategies for the modular ISOP Type D and modular IPOP Type D topologies is focused, aiming to achieve the desired control objectives. The next step involves selecting the suitable converter topology for each of the three stages of the modular Type D topology.

1.2.4 Stage-wise Topological Choices

The four feasible multilevel MVAC-MVDC topologies are neutral point clamped, flying capacitor converter, modular multilevel converter (MMC) and cascaded multilevel front end converter (CMFEC) [10, 19]. The first two are not suitable solutions as they do not facilitate easy scalability which is essential for plug-in and plug-out operation. MMC and CMFEC are the two most promising solutions for MVAC-MVDC conversion stage. While MMC offers the advantage of a single MVDC link for integrating MVDC sources/loads, it comes with drawbacks such as a very complex control system and the need for a bulky DC-side filter compared to CMFEC which significantly increases the cost. The CMFEC stands out as the most promising topology because of the simplicity of its modulation and control system. Hence, for the first stage of modular ISOP Type D SST, the CMFEC converter topology has been chosen in this research work.

In the second MVDC-LVDC stage, the converter houses the HF-link isolation transformer. This stage is regarded as one of the most challenging stages due to the high current on the LV side and the high voltage on the MV side. There are various feasible topology for the second stage. These are series LC resonsant converter (SRC), LLC resonant converter, dual half bridge (DHB) converter, dual active bridge converter (DAB), DAB with SRC, quad active bridge (QAB) converter [10, 19]. Out of these, the non-resonant DAB converter is selected in the second stage for this research work because it offers advantages such as: easily controllable bidirectional power flow by controlling the phase shift and a simple single phase shift (SPS) modulation scheme. Moreover, in DAB the efficiency can

be improved by adopting optimized modulation strategy like dual phase shift control (DPS) or triple phase shift control (TPS) or extended phase shift control (EPS).

The third stage is the LVDC-LVAC conversion stage for the load consumption side. A simple voltage source inverter is selected for the third stage. The circuit diagram of the selected modular ISOP Type D SST topology is shown in Fig. 1.9.

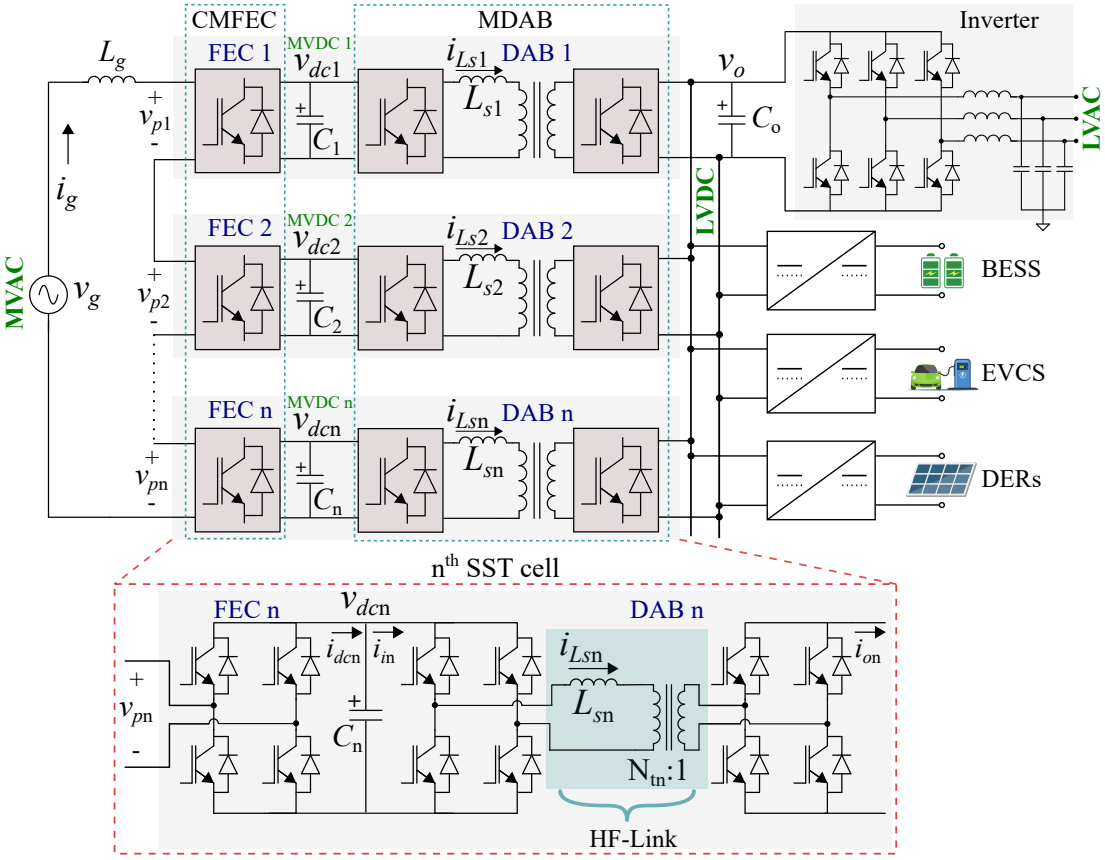


Figure 1.9: Selected three stage modular ISOP Type D SST topology.

1.3 Motivation of the Thesis

DAB is the central power processing unit of SST. It consists of two H-bridges, where both primary and secondary H-bridges are modulated at 50% duty cycle. The phase-shift-duty ratio, denoted by d_{φ}, between the two H-bridges is the control input to the plant which

controls the power flow. A state of art literature review on the control methods of a single cell DAB as well as in the context of modular SST is discussed subsequently.

1.3.1 Literature Review

DAB provides galvanic isolation through its HF-link consisting of an inductor and transformer. The magnitude of power transfer in the converter is predominantly governed by the fundamental component of this current. Meanwhile, its peak component dictates the over-current saturation boundary of the HF-link magnetic core. Hence, the information of this purely AC HF-link current is very important, which is missing while performing the single outer voltage loop control of DAB [28, 29, 30, 31]. The most widely used method for control of DAB is the dual loop control, which comprises an outer voltage loop and an inner current loop. The key features of the dual loop control strategy are: power flow control, limitation of current to provide over-current protection and improvement of the dynamic response of converter during load and line disturbances. The block diagram of dual loop control of DAB is shown in Fig. 1.10.

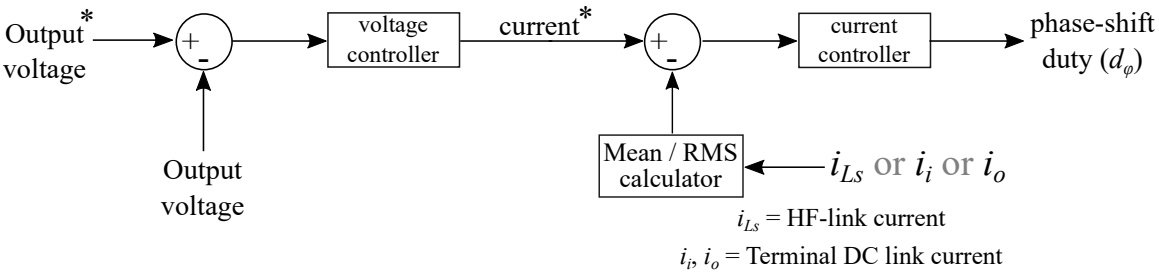


Figure 1.10: Dual loop control of DAB converter.

Dual loop control is proposed for the current stress optimization and efficiency improvement by deriving the optimal phase-shift-duty in [32, 33]. Predictive current mode control of DAB is presented in [34], which protects the transformer from saturation by measuring and sampling the HF-link current. A predicted peak-current based dual loop analog control of DAB is presented in [35] to achieve fast dynamic response for More

electric aircraft application. A double band analog current control method to avoid the risk of transformer saturation is proposed in [36] based on feed-forward compensation by measuring the HF-link current. Active saturation mitigation of DAB by detecting the variation of HF-link current slope near the saturation boundary is proposed in [37]. It depends on the measurement of the terminal DC-link current of DAB using current shunt resistor. Decoupled current control approach is employed in [38, 39], based on state observer to estimate and control the real and reactive power component independently. [38] requires HF-link AC current information, where as, [39] requires terminal DC link current information, which are obtained using different measurement techniques. However, these current measurements require high bandwidth current sensor, high sampling ADC and high sampling frequency. These challenges can be addressed by adopting current sensorless control utilizing estimation technique. The requirement of HF-link current estimation is discussed in detail in the subsequent subsection.

1.3.2 Requirement of HF-link Current Estimation

In order to implement dual loop control scheme, it is required to have the information of the HF-link current or the terminal DC-link current. The HF-link current and the terminal DC-link current are denoted by i_{hfac} and i_{tdc} respectively as shown in the Fig. 1.11. The HF-link current is a purely AC current whose fundamental frequency component is the switching frequency. The terminal DC-link current is a DC current with high ripple at twice the switching frequency. Fig. 1.11 illustrates the possible positions, denoted as P1, P2, and P3, where current sensors can be installed to measure the required current.

There are several types of current sensors/transducers based on their working principles and the technology used [40, 41]. For high power and high voltage application isolated current sensor is used. Few examples of commercially available isolated current sensors are shown in Fig. 1.12. The widely used method for measuring the terminal DC link current

is the combination of a shunt resistor and an optical isolation amplifier [37]. This approach offers several advantages, including cost-effectiveness, ease of handling and mounting. It is particularly well-suited for low current measurement. However, for applications involving high current, the shunt system faces several challenges. Magnetic IC current sensors are single chip solution used for the measurement of current over the PCB trace. However, these sensors have limited current measurement range and limited bandwidth. Rogoswski coil current sensing method features a thin and flexible design due to no use of mangetic core. It requires an integrator for the integration of output signal to obtain the actual current value. This integration process can introduce errors and inaccuracies in the measurement. Due to the use of air core it can also get affected by nearby magnetic field.

There are several types of magnetic core based current sensing methods, such as: current transformer, open loop Hall effect and closed loop Hall effect current sensor. The closed-loop Hall effect current sensor is favoured for high-current measurement applications. Its utilization of feedback compensation coil allows it to operate nearly at zero flux, resulting in significantly improved performance and accuracy. However, these are expensive and bulky. The magnetic core necessitates dedicated mounting space. Integrating this sensor on the busbar structure (as shown in positions P1, P3 of Fig. 1.11), may impede the goal of achieving a compact laminated busbar design to minimize stray inductance [42, 43].

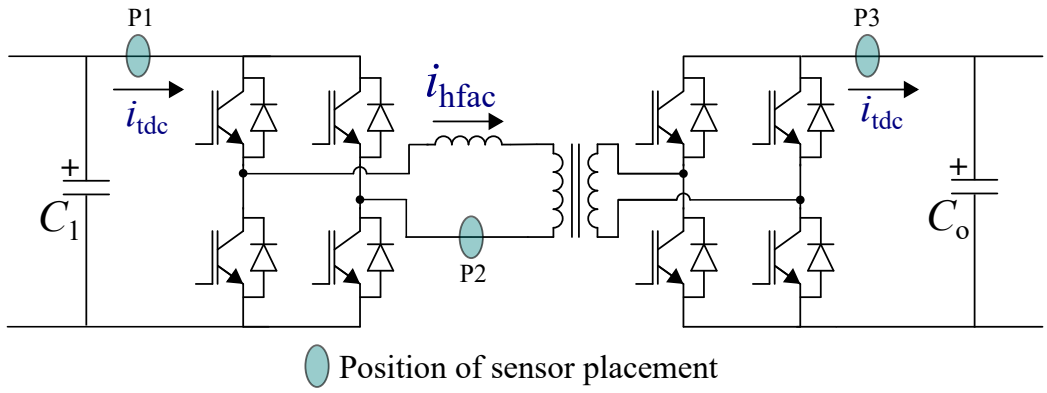


Figure 1.11: DAB circuit showing position of current sensor placement.

Apart from the HBW current sensor requirement, high sampling rate ADC is also essential to sample the current for digital control implementation. The sampling frequency must be nearly five to ten times greater than the switching frequency for signal processing, which imposes a limitation on the operating switching frequency of the DAB converter.

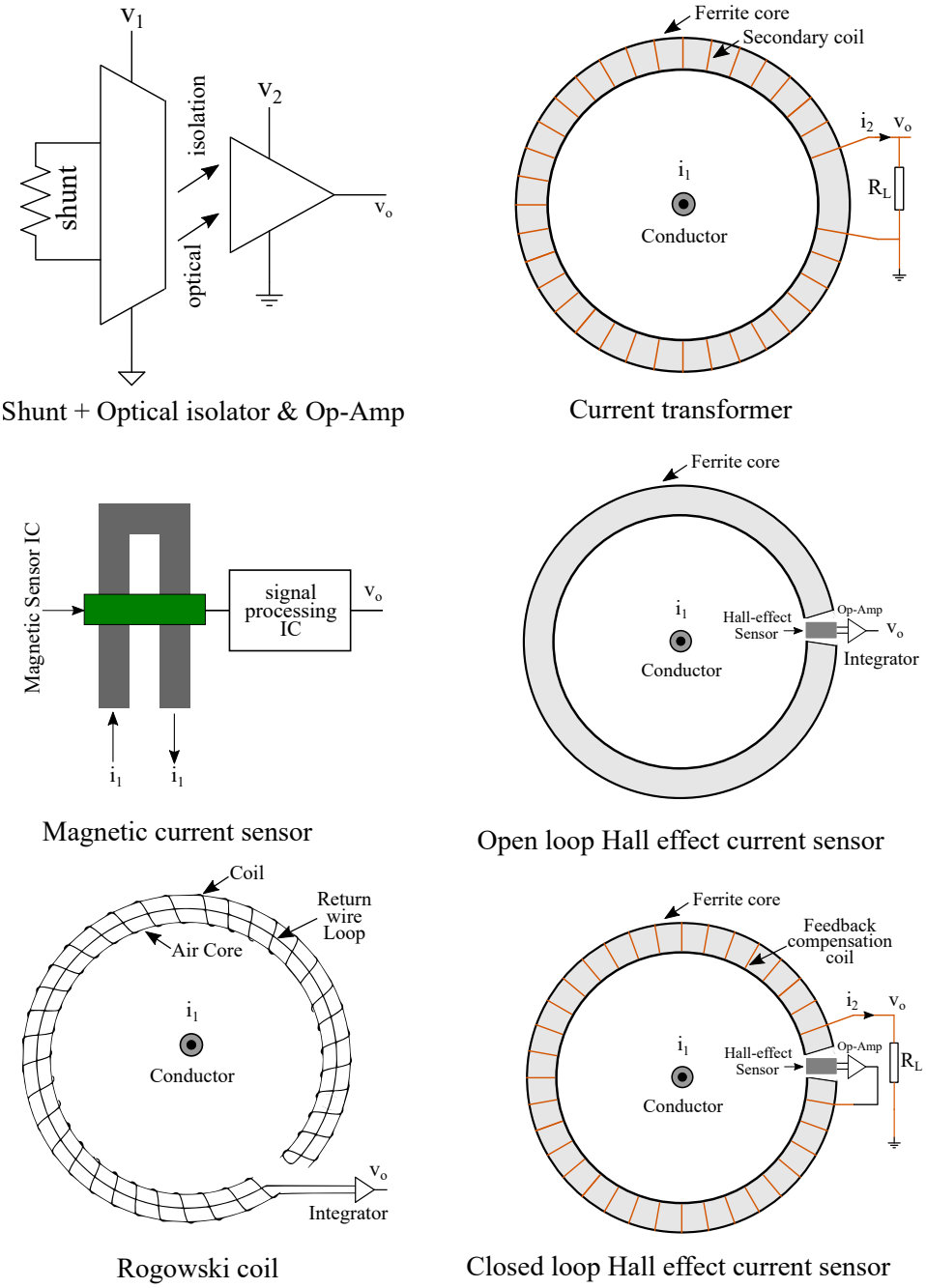


Figure 1.12: Few examples of isolated current sensors.

These above mentioned reasons stand as the principal motivation for implementing current sensorless control by estimation of the HF-link current.

1.3.3 Preservation of HF-Link Current Dynamics

Estimation of the HF-link current requires a well-defined dynamic model of the plant. Several modeling methods have been proposed to approximate the nonlinear and time-varying characteristics, in order to arrive at a linear, time-invariant representation. The three primary methodologies for modeling DAB converters are: discrete time modeling, reduced-order modeling and generalized average (GA) modeling. A full-order discrete-time modeling approach can have good accuracy and it is used for resonant converters. However, a simple continuous-time domain model is typically preferred due to its ability to offer more physical insights of the system. The reduced order model based on state space average modeling approach is commonly used for DAB. However, it does not include the dynamics of the HF-link current and hence does not provide any information regarding the HF-link current [44], [45].

In DAB, input voltage variation causes the HF-link current to transit from a trapezoidal shape to a more peaky waveform. When designing the inductor, its energy storing capability is determined by the peak current. However, as the peak current magnitude increases, the operating point moves closer to the knee region of B-H curve, which may lead to core saturation due to over-current. Estimating the HF-link current helps to gather information about its fundamental and peak magnitude. This is the reason for the estimation of HF-link current instead of the terminal DC-link current. The knowledge of the estimated fundamental current can be employed to control the active power. Besides this, monitoring the peak current aids in detecting over-current situations in the HF-link. This serves another motivation for the estimation of HF-link current with a good dynamic model which does not eliminate it as a state variable of the system. The GA modeling approach based on fun-

Table 1.2: Broad categorisation based on control strategy.

Strategy	Stage	Control Input	Balance Objective
A	CMFEC	Equal/unequal modulation-duty	MVDC balance
	DAB	Phase-shift-duty	Power balance
B	CMFEC	Only equal modulation-duty	MVDC balance
	DAB	Phase-shift-duty	Power balance
C	CMFEC	Only equal modulation-duty	- - -
	DAB	Phase-shift-duty	MVDC & Power balance

damental harmonic approximation (FHA) helps in capturing the dynamics of the HF-link current and its low frequency envelope. This thesis aims to utilize the Generalized Average (GA) model and develop an estimator which can capture the dynamics of HF-link current.

1.3.4 Extension of Control Scheme to Modular Structure

The adoption of the modular configuration in high-power applications is due to its numerous advantages, as discussed earlier. Nevertheless, the modular structure faces challenges arising from cell-to-cell parametric variation caused by manufacturing errors and ageing related factors. In a modular SST, the HF-link inductance of the DAB converter plays a pivotal role in governing the power flow between cells. The variation of this parameter among the cells is the primary cause of power imbalances across the different cells of the modular SST.

There are various voltage and power balance methods proposed to tackle this problem. According to the control objectives of CMFEC in the first stage and modular DAB in the second stage, the control strategies can be categorized broadly into three types, which are: Strategy A , Strategy B and Strategy C.

The control objectives of strategy A in CMFEC stage are: grid side unity power factor operation, regulation of summation of MVDC voltages and MVDC voltage balance [46,

47]. The role of modular DAB is to regulate the LVDC port voltage and balance cell-to-cell power. The limitation of this approach is, it requires the measurement of HF-link current or terminal DC link current using high HBW current sensors and high sampling ADCs to calculate average power for the implementation of power balance control.

Strategy B balance control approach is also proposed without measuring the HF-link current [48, 49] by modifying the active component of CMFEC duty ratio. Current sensorless power balance control strategy of SST is proposed to eliminate the use of HBW current sensor using strategy C. This method draws inspiration from the common control approach utilized for ISOP DC-DC converters [50, 51, 52]. Since modular SST is an ISOP AC-DC converter, this method is adopted by assigning a common modulation-duty cycle to all series connected FECs of CMFEC [53, 54, 55, 56]. This effectively ensures that all output parallel connected modular DAB behaves like ISOP DC-DC converter enabling power balance across the modular SST. In the modular DAB stage using the MVDC voltage balance controller the phase-shift-duty in each DAB is compensated to achieve power balance. Hence, the control objective of modular DAB is both MVDC voltage balance and cell-to-cell power balance. The CMFEC does not participate in any balance objective. It only regulates MVDC voltage summation and achieve grid side UPF operation. When it comes to control mechanism, strategy B is similar to strategy C eventually in the steady state. In both control approach, the modular DAB converter functions as equivalent to ISOP system.

Due to the possibility of only common modulation-duty in CMFEC stage in both strategy B and C control approach, it puts constraints on utilization of the full degrees of freedom provided by the topology. It does not allow cell-to-cell current control. A major drawback is its inability to provide controlled unequal power sharing capability. In modular configurations, controlled unequal power sharing can yield several advantages, particularly in facilitating phase shedding and addition operations (plug-in and plug-out operation) to enhance overall system efficiency during low load periods. Additionally, these schemes

are only applicable to ISOP configurations and they fall short in achieving power balance in IPOP configurations. The reasons mentioned above serve as the primary motivation for developing a flexible power sharing control strategy based on HF-link current estimation and parameter identification, which can be adopted for any configuration. Therefore, the broad aim of the thesis is categorized into the following.

1.4 Objectives of the Thesis

The objectives of this thesis are,

1. Development of a HBW current sensorless control scheme for single cell DAB, which provides a direct control handle on the HF-link current fundamental envelope, enabling the control over its active power.

2. Utilizing the developed control scheme, develop a control strategy to achieve the flexible power sharing of modular ISOP SST, which can offer controlled equal, unequal and zero power sharing feature.

3. Utilizing the developed control scheme, develop a control strategy to achieve the flexible power sharing of modular IPOP AC-DC converter for high-input-high-output current application.

4. Perform experimental validations of the analytical claims.

1.5 Thesis Outline

A pictorial representation of the thesis highlighting its key contributions and its outline is presented in Fig. 1.13. This thesis is organized in to six chapters in the following manner.

- **Chapter 2** focuses on the dynamic modeling approach and modulation schemes employed for SST in this research work. This chapter covers the derivation of the low-frequency dynamic model of the CMFEC and presents its Pulse Width Modulation (PWM) scheme. Additionally, the modeling strategies of the DAB converter and its modulation strategy are also discussed.

- **Chapter 3** proposes a hierarchical control scheme for a single cell DAB converter. This control strategy focuses on regulating the fundamental and peak component of the HF-link current without using high bandwidth sensors. Relevant experimental results are presented for the validation.

- **Chapter 4** presents a voltage and power control strategy for modular SST, which, in addition to enabling cell-to-cell power balance, also offers controlled flexible power sharing when needed by controlling the HF-link fundamental current component. Relevant experimental results are presented for the validation.

- **Chapter 5** introduces a control strategy that achieves voltage balance and flexible power sharing for modular IPOP AC-DC converters with HF-link isolation. The UPF operation of multiple parallel cells on the grid side is performed using only one current sensor, while parameter identification is conducted through perturbation algorithm. Relevant experimental results are presented for the validation.

- **Chapter 6** concludes this thesis by summarizing its key findings and identifying several potential directions for future research.

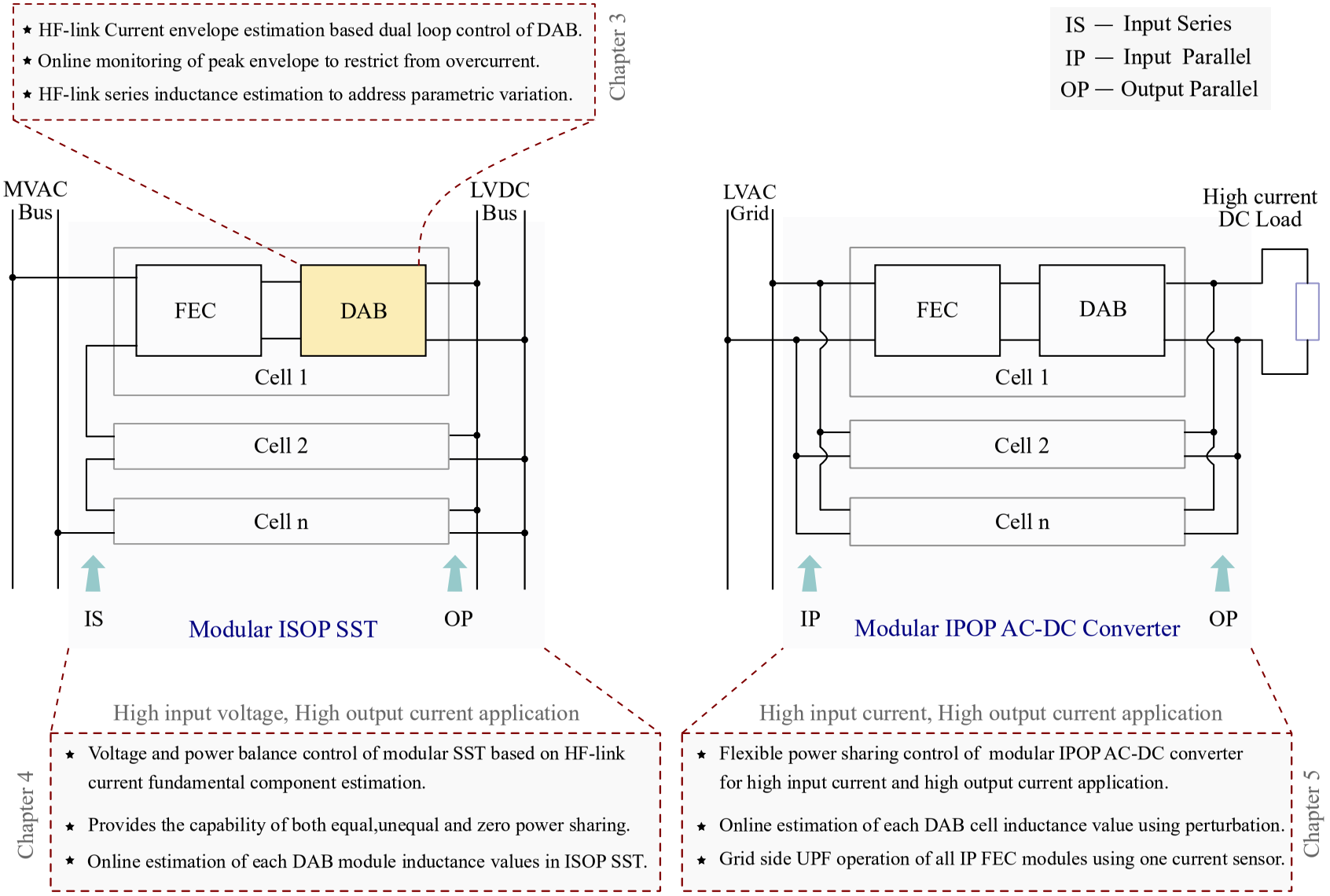
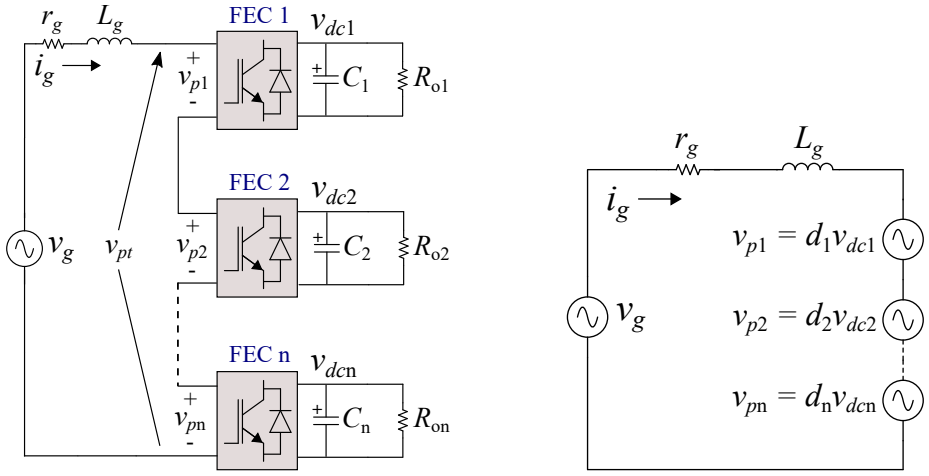


Figure 1.13: A pictorial representation highlighting key research contributions and outline of this thesis.

Chapter 2

Low Frequency Dynamic Model

In this chapter, the low-frequency linear dynamic model of SST is presented. The modeling process is divided into two distinct steps: AC-DC CMFEC stage and DC-DC isolation OPDAB stage, which are discussed sequentially. The primary objective of this chapter is to derive the average large signal model, the linearized small signal model and key control-input-to-state-variable transfer functions for each stages. The pulse width modulation (PWM) schemes employed in this research work are also discussed.



(a) CMFEC circuit diagram. **(b)** AC equivalent circuit.

Figure 2.1: CMFEC and its AC equivalent circuit.

2.1 Modeling of CMFEC

The control objectives of the CMFEC stage are

1. To draw unity power factor from the grid.
2. To regulate the summation of all MVDC voltages.
3. To regulate and balance the individual MVDC voltage. (if MVDC voltage balance control objective is adopted in this stage - Strategy A).

The circuit diagram of the CMFEC stage and its AC equivalent circuit is shown in Fig. 2.1. The dynamic equations of CMFEC averaged over a switching period are,

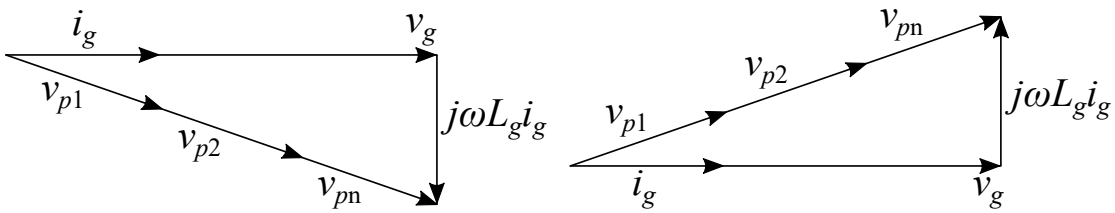
$$\frac{di_g}{dt} = \frac{v_g}{L_g} - \frac{r_g}{L_g} i_g - \frac{v_{pt}}{L_g}, \tag{2.1}$$

$$\frac{dv_{dck}}{dt} = \frac{i_{dck}}{C_k} - \frac{i_{ik}}{C_k} = \frac{d_k i_g}{C_k} - \frac{1}{C_k}\frac{v_{dck}}{R_{ok}}, \text{where} \quad k = 1, 2..., n. \tag{2.2}$$

Here, the grid voltage, grid current, and the k^{th} cell MVDC voltage are denoted by v_g, i_g and v_{dck} respectively. The parasitic resistance of grid interfacing inductance (L_g) is r_g and C_k is the MVDC capacitance of k^{th} cell . R_{ok} is the effective input impedance of k^{th} DAB, which behaves as a load to the k^{th} FEC. The total pole voltage (v_{pt}) is given in (2.3), where, d_k is the modulation-duty ratio of k^{th} FEC module.

$$v_{pt} = \sum_{k=1}^{n} v_{pk} = \sum_{k=1}^{n} d_k v_{dck}. \tag{2.3}$$

The phasor diagram of CMFEC for forward and reverse power flow is shown in Fig. 2.2 . v_g and i_g are required to be in phase for UPF operation. To meet this objective, the conventional vector control method is adopted. The stationary orthogonal axes $\alpha\beta$ are



(a) Forward power flow. **(b)** Reverse power flow.

Figure 2.2: Phasor diagram of CMFEC for UPF operation.

transformed into synchronously rotating dq reference frame. It is presented in Fig. 2.3. The dynamic equations of CMFEC in dq reference frame are derived as,

$$\frac{di_{gd}}{dt} = \frac{v_{gd}}{L_g} - \frac{r_g}{L_g} i_{gd} + \omega i_{gq} - \frac{1}{L_g} \sum_{k=1}^{n} d_{dk} v_{dck}, \tag{2.4}$$

$$\frac{di_{gq}}{dt} = \frac{v_{gq}}{L_g} - \frac{r_g}{L_g} i_{gq} - \omega i_{gd} - \frac{1}{L_g} \sum_{k=1}^{n} d_{qk} v_{dck}, \tag{2.5}$$

$$\frac{dv_{dck}}{dt} = \frac{1}{C_k}[d_{dk} i_{gd} + d_{qk} i_{gq}] - \frac{i_{ik}}{C_k}; \quad k = 1, 2..., n., \tag{2.6}$$

where, x_d and x_q represent the d and q axis component of x, $x \in [v_g, i_g, d_k]$. The small signal model is derived by applying a small perturbation to the control input d_k in the dq domain as,

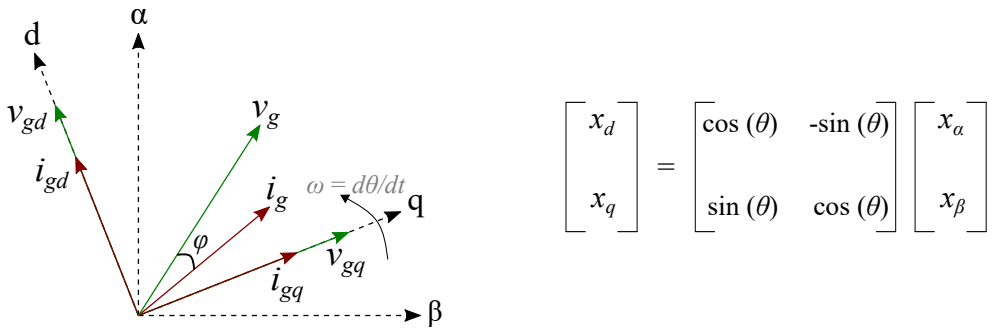


Figure 2.3: Stationary $\alpha\beta$ to synchronously rotating dq reference frame transformation.

$$\tilde{d}_{dk} = d_{dk} - D_{dk}, \tag{2.7}$$

$$\tilde{d}_{qk} = d_{qk} - D_{qk}, \tag{2.8}$$

where, the $\tilde{d}_{dk}$, $\tilde{d}_{qk}$ are the control inputs and D_{dk}, D_{qk} are the steady state values at the operating point of linearization. The perturbation in control input will cause deviation in the state variable x, $x \in [v_g, i_g, v_{dck}]$. The perturbed and steady state value of variable x are $\tilde{x}$ and X respectively. Consequently, the linearised small signal model is derived as,

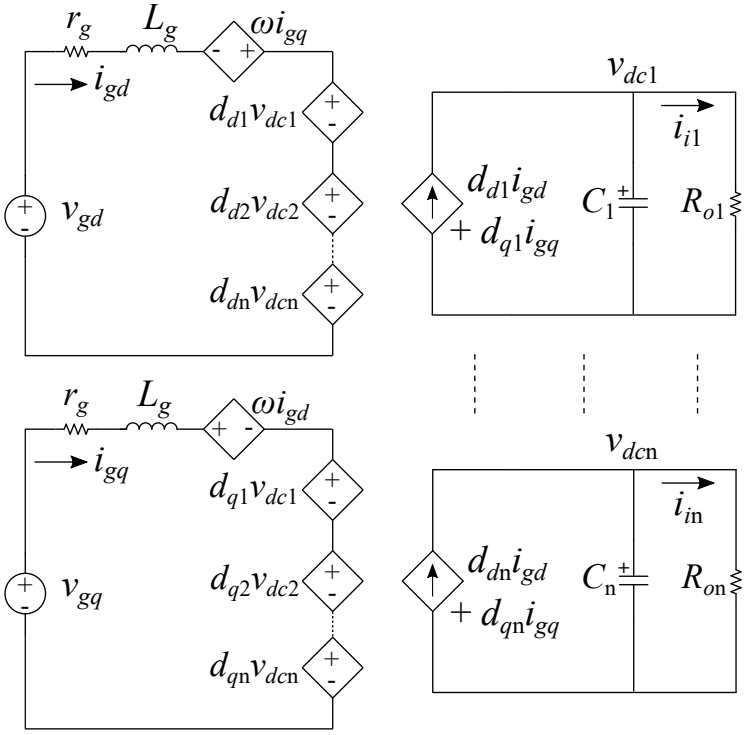
$$\frac{d\tilde{i}_{gd}}{dt} = \frac{\tilde{v}_{gd}}{L_g} - \frac{r_g}{L_g}\tilde{i}_{gd} + \omega\tilde{i}_{gq} - \frac{1}{L_g}\left[\sum_{k=1}^{n} \tilde{d}_{dk}V_{dck} + \sum_{k=1}^{n} D_{dk}\tilde{v}_{dck}\right], \tag{2.9}$$

$$\frac{d\tilde{i}_{gq}}{dt} = \frac{\tilde{v}_{gq}}{L_g} - \frac{r_g}{L_g}\tilde{i}_{gq} - \omega\tilde{i}_{gd} - \frac{1}{L_g}\left[\sum_{k=1}^{n} \tilde{d}_{qk}V_{dck} + \sum_{k=1}^{n} D_{qk}\tilde{v}_{dck}\right], \tag{2.10}$$

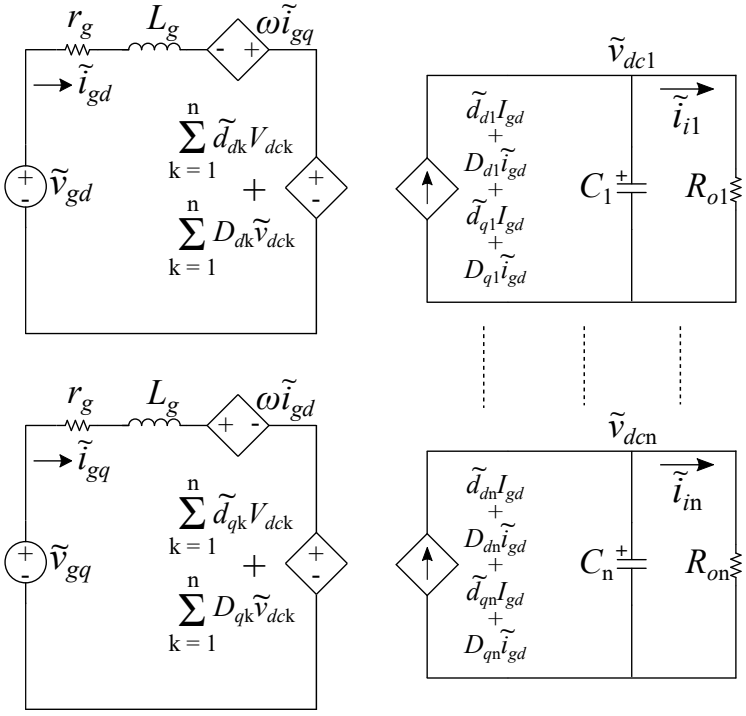
$$\frac{d\tilde{v}_{dck}}{dt} = \frac{1}{C_k}[\tilde{d}_{dk}I_{gd} + D_{dk}\tilde{i}_{gd} + \tilde{d}_{qk}I_{gq} + D_{qk}\tilde{i}_{gq}] - \frac{\tilde{i}_{ik}}{C_k}, \text{where} \quad k = 1, 2..., n. \tag{2.11}$$

The large signal and the small signal model circuit diagram of CMFEC in dq reference frame is shown in Fig. 2.4. For the derivation of transfer functions from the small signal model, the cross coupling terms ($+\omega\tilde{i}_{gq}$ and $-\omega\tilde{i}_{gd}$) are not considered as their effect will be compensated through the inclusion of decoupling feed-forward terms in the closed-loop control. The control-to-output current ($G_{igd-ddk}, G_{igq-dqk}$), current-to-output voltage ($G_{vdck-igd}, G_{vdck-igq}$) and control-to-output voltage ($G_{vdck-ddk}, G_{vdck-dqk}$) transfer functions are derived and shown as follows,

$$G_{igd-ddk}(s) = \frac{\tilde{i}_{gd}(s)}{\tilde{d}_{dk}(s)} = -\frac{V_{dck}}{sL_g + r_g}, \qquad G_{igq-dqk}(s) = \frac{\tilde{i}_{gq}(s)}{\tilde{d}_{qk}(s)} = -\frac{V_{dck}}{sL_g + r_g}. \tag{2.12}$$



(a) Large signal model.



(b) Linearised small signal model.

Figure 2.4: Large signal and small signal model of CMFEC in dq reference frame.

$$G_{vdck-igd}(s) = \frac{\tilde{v}_{dck}(s)}{\tilde{i}_{gd}(s)} = \frac{D_{dk}R_{ok}}{sC_kR_{ok}+1}, \quad G_{vdck-igq}(s) = \frac{\tilde{v}_{dck}(s)}{\tilde{i}_{gq}(s)} = \frac{D_{qk}R_{ok}}{sC_kR_{ok}+1}. \tag{2.13}$$

$$G_{vdck-ddk}(s) = \frac{\tilde{v}_{dck}(s)}{\tilde{d}_{dk}(s)} = \frac{I_{gd}R_{ok}}{sC_kR_{ok}+1}, \quad G_{vdck-dqk}(s) = \frac{\tilde{v}_{dck}(s)}{\tilde{d}_{dq}(s)} = \frac{I_{gq}R_{ok}}{sC_kR_{ok}+1}. \tag{2.14}$$

Utilizing these transfer functions, the closed loop control diagram of CMFEC is shown in Fig. 2.5. It is a dual loop control consisting of outer voltage loop and inner current loop. H_{vs} and H_{ig} represents the voltage controller and current controller for the outer loop and inner loop respectively. The feed-forward terms ($i_{gd}C_1$, $i_{gq}C_1$ and $v_{gd}C_2$) are added to the inner current loop for decoupled current control. The load disturbance input of the k^{th} cell is denoted by i_{dtbk}. The actuator transfer function of k^{th} FEC (G_{actk}) is given in (2.15), where, T_d is the switching period delay using Padé approximation.

$$G_{actk} = \frac{V_{dck}}{1+sT_d}. \tag{2.15}$$

For the UPF operation v_g can be aligned on the d-axis using phase locked loop (PLL), which will make its q-axis component zero ($v_{gq} = 0$). For UPF operation the inner current reference i^*_{gq} can be set as zero. This will make the reactive power drawn by SST from the grid equal to zero. Δd_{dk} is the modification in the modulation-duty cycle of k^{th} FEC generated from the voltage balance controller. The working of the voltage balance controller is not presented here. This will be discussed in detail in chapter 4.

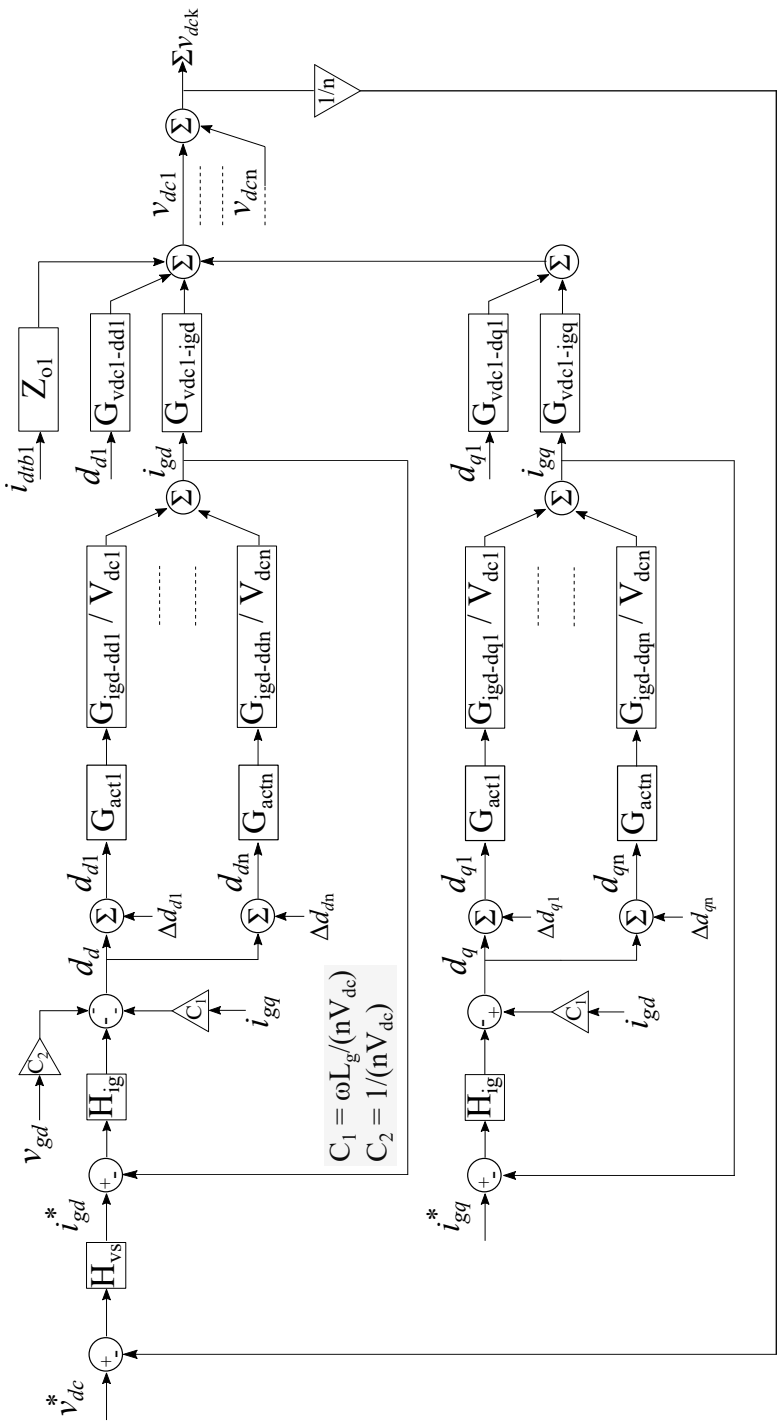


Figure 2.5: Control diagram of CMFEC in dq reference frame showing dual loop control.

2.2 Modulation Scheme of CMFEC

The most widely used PWM strategy for CMFEC is the multi-carrier PWM technique. Each carrier signal is assigned to a particular H-bridge of CMFEC, which has to be modulated independently using either bipolar or unipolar PWM. In bipolar PWM, each H-bridge produces two-level pole voltages ($+v_{dc}$, $-v_{dc}$), whereas in unipolar PWM, it generates 3-level pole voltages ($+v_{dc}$, 0, $-v_{dc}$). Unipolar PWM has the advantage of lower dv/dt transitions compared to bipolar PWM. In the unipolar PWM method, the dominant switching frequency harmonics are centered at a position that is two times farther compared to bipolar PWM. This results in lower THD in the pole voltages for unipolar PWM.

When there are n cells connected in series with each H-bridge of CMFEC can generating a 3-level individual pole voltage, a total input pole voltage (v_{pt}) of maximum $2n + 1$ levels can be synthesized. This multilevel operation is achieved by interleaving the carrier signals. If there are n number of cells, each carrier is phase shifted by an angle of $360^0/n$. Interleaving the carrier signals leads to an apparent switching frequency of $2nf_{FEC}$ seen by the grid, where f_{FEC} is the switching frequency of each FEC H-bridge. This helps in achieving a lower THD in the grid current to meet the required grid standards. The dynamic model of the OPDAB is derived sequentially.

2.3 Modeling of OPDAB

The control objectives of the OPDAB stage are,

1. To regulate the output LVDC voltage v_o.
2. To achieve equal throughput power sharing among the cells.
3. To regulate and balance the individual MVDC voltage. (if MVDC voltage balance control objective is adopted in this OPDAB stage - Strategy B).

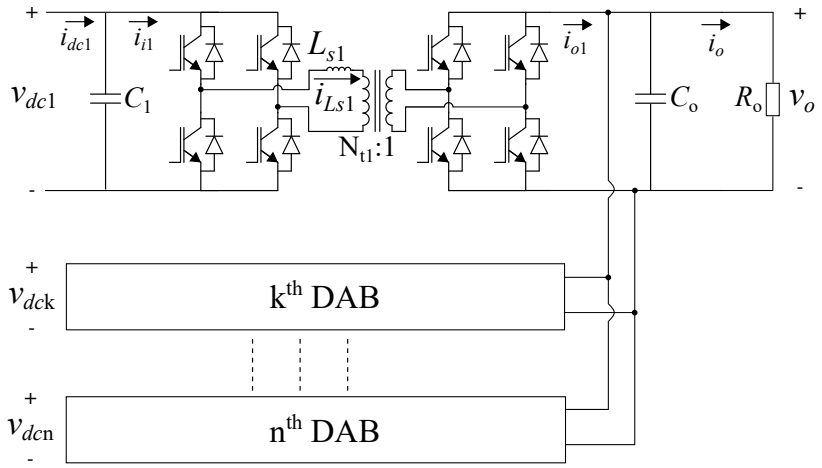


Figure 2.6: Modular OPDAB circuit diagram.

2.3.1 Reduced Order Modeling

The circuit diagram of the OPDAB stage is shown in Fig. 2.6. The dynamic equations governing the input and output voltages of the DAB converter are,

$$\frac{dv_{dck}}{dt} = \frac{1}{C_k}(i_{dck} - i_{ik}), \qquad k = [1, 2...n], \tag{2.16}$$

$$\frac{dv_o}{dt} = \frac{1}{C_o}\left[\left(\sum_{k=1}^{n} i_{ok}\right) - i_o\right]. \qquad k = [1, 2...n]. \tag{2.17}$$

C_k is the input capacitor of k^{th} DAB module and C_o is the output capacitor. The input and output DC link current of k^{th} DAB are denoted by i_{ik} and i_{ok} respectively. The output DC link current of k^{th} FEC module is i_{dck}. The load current is denoted by i_o. The instantaneous throughput power transfer equation of k^{th} DAB module with single phase shift (SPS) modulation scheme is,

$$p_k = v_{dck}i_{ik} = v_o i_{ok} = \frac{N_{tk}}{2f_s L_{sk}} d_{\varphi k}(1 - d_{\varphi k}) v_o v_{dck}, \tag{2.18}$$

where N_{tk}, L_{sk} and f_s are the HF-link turns ratio, inductance value and the switching

frequency of k^{th} DAB respectively. $d_{\varphi k}$, the phase-shift-duty-ratio between the two H-bridges, is the control input to the k^{th} DAB. The expression for i_{ik} and i_{ok} are derived from (2.18) and are presented in (2.19) and (2.20).

$$i_{ik} = \frac{N_{tk}}{2f_s L_{sk}} d_{\varphi k}(1 - d_{\varphi k}) v_o. \tag{2.19}$$

$$i_{ok} = \frac{N_{tk}}{2f_s L_{sk}} d_{\varphi k}(1 - d_{\varphi k}) v_{dck}. \tag{2.20}$$

The small signal model is derived by applying a small perturbation to the control input $d_{\varphi k}$ as,

$$\tilde{d}_{\varphi k} = d_{\varphi k} - D_{\varphi k}, \tag{2.21}$$

where, the $\tilde{d}_{\varphi k}$ is the perturbed control input and $D_{\varphi k}$ is its steady state value. The perturbed and steady state value of variable y are $\tilde{y}$ and Y respectively. The resulting small signal equations of the OPDAB stage are given in (2.22) and (2.23). The linearized $\tilde{i}_{ik}$ and $\tilde{i}_{ok}$ can be derived using (2.19), (2.20) and (2.21) respectively.

$$\frac{d\tilde{v}_{dck}}{dt} = \frac{1}{C_k}(\tilde{i}_{dck} - \tilde{i}_{ik}), \tag{2.22}$$

$$\frac{d\tilde{v}_o}{dt} = \frac{1}{C_o}\left[\left(\sum_{k=1}^{n} \tilde{i}_{ok}\right) - \tilde{i}_o\right], \tag{2.23}$$

$$\tilde{i}_{ik} = \frac{N_{tk}}{2f_s L_{sk}} D_{\varphi k}(1 - D_{\varphi k})\tilde{v}_o + \frac{N_{tk}}{2f_s L_{sk}} V_o(1 - 2D_{\varphi k})\tilde{d}_{\varphi k}. \tag{2.24}$$

$$\tilde{i}_{ok} = \frac{N_{tk}}{2f_s L_{sk}} D_{\varphi k}(1 - D_{\varphi k})\tilde{v}_{dck} + \frac{N_{tk}}{2f_s L_{sk}} V_{dck}(1 - 2D_{\varphi k})\tilde{d}_{\varphi k}. \tag{2.25}$$

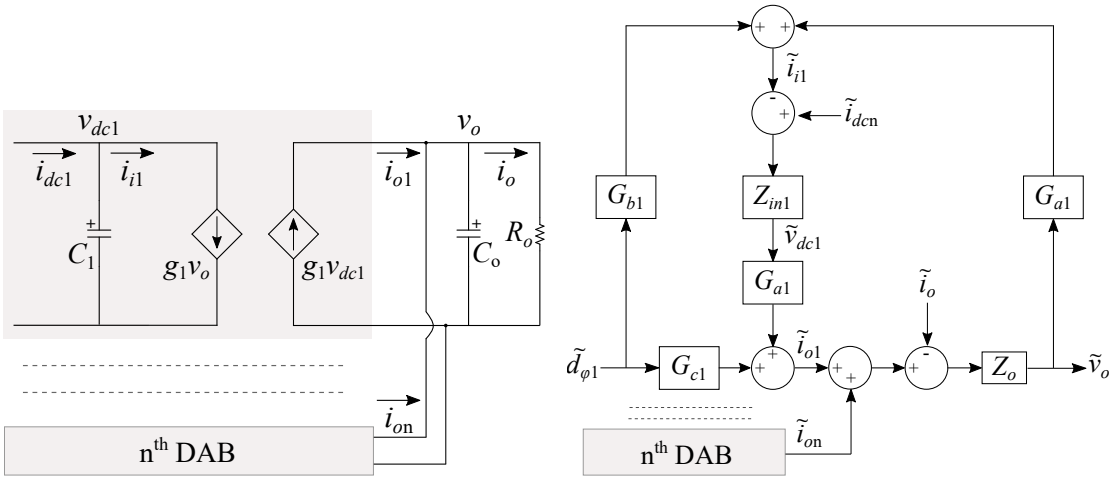
The input impedance Z_{ink} and the output impedance Z_o are shown in (2.26). The large

signal and the small signal model circuit diagram of OPDAB stage is shown in Fig. 2.7.

$$Z_{ink} = \frac{1}{sC_k}, \quad Z_o = \frac{R_o}{1 + sC_o}. \tag{2.26}$$

The gains G_{ak}, G_{bk} and G_{ck} are expressed as,

$$G_{ak} = \frac{N_{tk}}{2f_s L_{sk}} D_{\varphi k}(1 - D_{\varphi k}),\ G_{bk} = \frac{N_{tk}}{2f_s L_{sk}} V_o(1 - 2D_{\varphi k}),\ G_{ck} = \frac{N_{tk}}{2f_s L_{sk}} V_{dck}(1 - 2D_{\varphi k}). \tag{2.27}$$



(a) OPDAB large signal model. **(b)** Linearised small signal model.

Figure 2.7: Large signal and small signal model of OPDAB stage.

This modeling approach is commonly known as reduced order modeling, as it considers only the capacitor voltages (v_{dck} and v_o) as the state variables of the system. The shortcoming of this modeling approach is its inability to consider i_{Lsk} as the state variable.

2.3.2 Generalized Average Model

The conventional state-space averaging technique requires negligible switching ripple in the waveform while modeling DC-DC converter. However, in the case of DAB converters, this requirement is not met due to the purely AC nature of the transformer current. Con-

sequently, the generalized averaging (GA) technique emerges as a viable alternative which incorporates dominant terms in the Fourier series of state variables [44], [45]. GA method effectively captures the influence of pure AC current i_{Lsk} on converter dynamics.

The gate drive signals of IGBT switches, primary bridge pole voltage (v_{prin}), secondary bridge pole voltage (v_{secn}), voltage across inductor (v_{Lsn}) and inductor current (i_{Lsn}) waveforms of n^{th} DAB converter during one switching period are shown in Fig. 2.8. The parasitic resistance (on state IGBT switch resistance, HF-link transformer winding resistance and HF-link inductor parasitic resistance) are lumped together and denoted by R_{sn}. For a DAB with SPS modulation scheme, the primary H-bridge pole voltage of n^{th} DAB module, $(v_{prin}(\tau))$ is given by,

$$v_{prin}(\tau) = s_{prin}(\tau) v_{dcn}(\tau) \tag{2.28}$$

where the switching function of primary bridge $(s_{prin}(\tau))$ is defined as,

$$s_{prin}(\tau) = \begin{cases} +1, & 0 \leq \tau < \dfrac{T}{2} \\ \\ -1, & \dfrac{T}{2} \leq \tau < T \end{cases} \tag{2.29}$$

where $T = \dfrac{1}{f_s}$ and $\omega = 2\pi f_s$. The total time span for this analysis is represented by τ and it is referenced to the rising edge of s_{prin} where $t = 0$. Similarly, the secondary bridge side pole voltage, $(v_{secn}(\tau))$, is given by

$$v_{secn}(\tau) = s_{secn}(\tau) v_o(\tau). \tag{2.30}$$

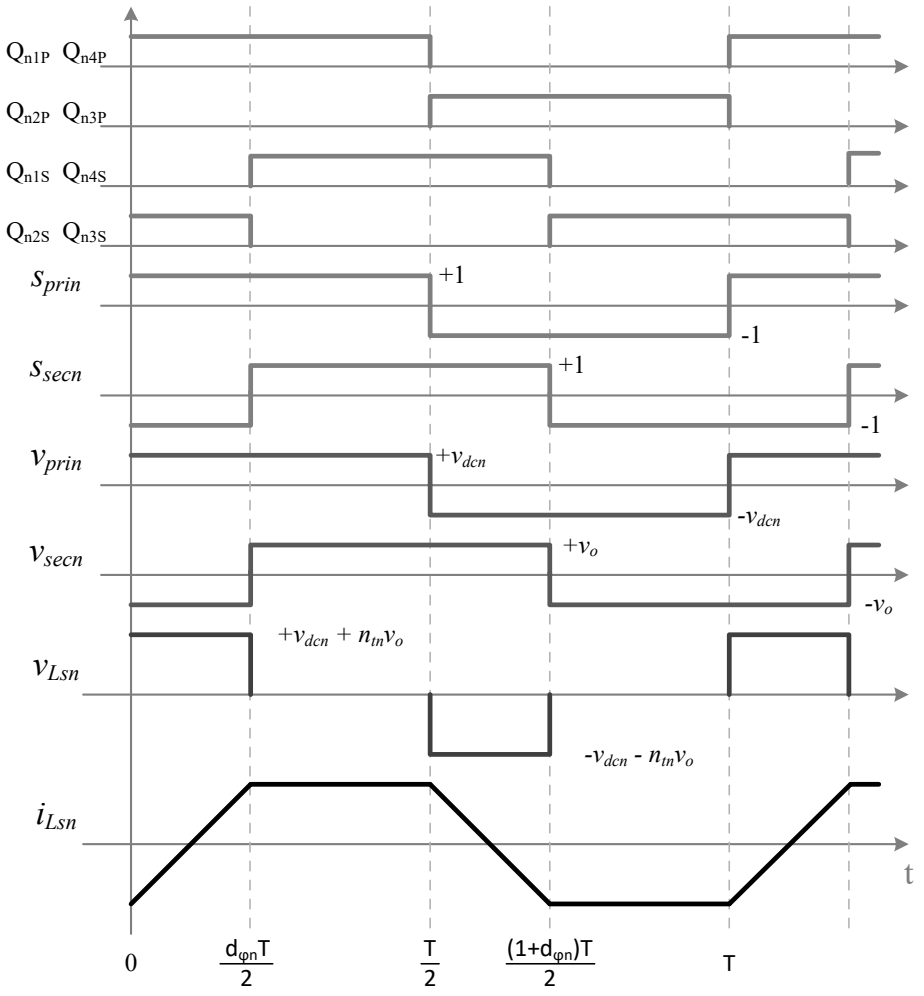


Figure 2.8: DAB waveforms during one switching period

$(s_{secn}(\tau))$ denotes the switching function of the secondary bridge, where,

$$s_{secn}(\tau) = \begin{cases} +1, & \dfrac{d_{\varphi n}T}{2} \leq \tau < \dfrac{(1+d_{\varphi n})T}{2} \\ -1, & \dfrac{(1+d_{\varphi n})T}{2} \leq \tau < \dfrac{d_{\varphi n}T}{2} + T. \end{cases} \tag{2.31}$$

While deriving the dynamic equations, it is assumed that the power balance is achieved in the modular SST for simplicity. Considering the output capacitor voltage (v_o), input capacitor voltage (v_{dcn}) and inductor current (i_{Lsn}), as the three state variables of the n^{th}

DAB, the large signal dynamic equations can be derived as,

$$\frac{dv_o(\tau)}{dt} = -\frac{i_o(\tau)}{C_o} + \frac{ni_{on}(\tau)}{C_o} = -\frac{1}{R_oC_o}v_o(\tau) + \frac{nN_{tn}s_{secn}(\tau)}{C_o}i_{Lsn}(\tau), \tag{2.32}$$

$$\begin{aligned}\frac{di_{Lsn}(\tau)}{dt} &= -\frac{R_{sn}}{L_{sn}}i_{Lsn}(\tau) + \frac{v_{prin}(\tau)}{L_{sn}} - \frac{N_{tn}v_{secn}(\tau)}{L_{sn}} \\ &= -\frac{R_{sn}}{L_{sn}}i_{Lsn}(\tau) + \frac{s_{prin}(\tau)}{L_{sn}}v_{dcn}(\tau) - \frac{N_{tn}s_{secn}(\tau)}{L_{sn}}v_o(\tau),\end{aligned} \tag{2.33}$$

$$\frac{dv_{dcn}(\tau)}{dt} = \frac{i_{dcn}(\tau)}{C_n} - \frac{i_{in}(\tau)}{C_n} = \frac{1}{C_n}i_{dcn}(\tau) - \frac{s_{prin}(\tau)}{C_n}i_{Lsn}(\tau), \tag{2.34}$$

The next step is to average the dynamic equations using generalized average (GA) method [44, 45]. In GA modeling approach this averaging is done by representing a state variable, $x(\tau)$, during the time interval $\tau \in [t-T,\, t]$, using the complex Fourier series (FS) representation,

$$x(\tau) = \sum_{k=-\infty}^{\infty} \langle x \rangle_k(t) e^{jk\omega\tau}, \tag{2.35}$$

where, $\langle x \rangle_k(t)$ is k^{th} complex Fourier coefficient (FC) of $x(\tau)$ and it is given by,

$$\langle x \rangle_k(t) = \frac{1}{T}\int_{\tau=(t-T)}^{t} x(\tau)e^{-jk\omega\tau}d\tau = \frac{1}{T}\int_{\tau=(t-T)}^{t} x(\tau)\Big(\cos k\omega\tau - j\sin k\omega\tau\Big)d\tau. \tag{2.36}$$

A low d_φ is advisable for lower conduction losses for the same throughput power. For low d_φ, the inductor current is dominated by its fundamental component. Similarly the DC component is predominant in the DC-link voltages due to negligible switching ripple in them. Hence, the fundamental component (-1^{st}, 1^{st}) and DC component (0^{th}) in the complex FS expansion of state variables are considered in this analysis for simplicity. Model accuracy can be increased by considering more FCs without neglecting them. However, the complexity increases with inclusion of more FCs. Hence, considering only -1^{st}, 0^{th} and 1^{st} FCs of x and y, from (A.7) it can be derived as,

$$\langle xy\rangle_1 = \langle x\rangle_1\langle y\rangle_0 + \langle x\rangle_0\langle y\rangle_1 \tag{2.37}$$

$$\langle xy\rangle_{-1} = \langle x\rangle_{-1}\langle y\rangle_0 + \langle x\rangle_0\langle y\rangle_{-1} \tag{2.38}$$

$$\langle xy\rangle_0 = \langle x\rangle_0\langle y\rangle_0 + \langle x\rangle_{-1}\langle y\rangle_1 + \langle x\rangle_1\langle y\rangle_{-1} \tag{2.39}$$

In the above expressions, ($\langle x\rangle_1$, $\langle x\rangle_{-1}$) and ($\langle y\rangle_1$, $\langle y\rangle_{-1}$) are fundamental component complex conjugates. $\langle x\rangle_0$ and $\langle y\rangle_0$ represent the 0^{th} FC/average DC value of x and y states. Solving (2.37), (2.38) and (2.39), the fundamental component real part ($\langle xy\rangle_1^R$, imaginary part ($\langle xy\rangle_1^I$) and the DC component ($\langle xy\rangle_0$) can be derived as,

$$\langle xy\rangle_1^R = \langle x\rangle_1^R\langle y\rangle_0 + \langle x\rangle_0\langle y\rangle_1^R, \tag{2.40}$$

$$\langle xy\rangle_1^I = \langle x\rangle_1^I\langle y\rangle_0 + \langle x\rangle_0\langle y\rangle_1^I, \tag{2.41}$$

$$\langle xy\rangle_0 = \langle x\rangle_0\langle y\rangle_0 + 2\big[\langle x\rangle_1^R\langle y\rangle_1^R + \langle x\rangle_1^I\langle y\rangle_1^I\big]. \tag{2.42}$$

Here, $\langle x\rangle_1^R$ and $\langle y\rangle_1^R$ represent the real part of the fundamental component of x and y. Similarly, $\langle x\rangle_1^I$ and $\langle y\rangle_1^I$ represent the imaginary part of the fundamental component of x and y. Subsequently, applying (A.4), (2.40), (2.41) and (2.42) to the dynamic equations in (2.32), (2.33) and (2.34) the 0^{th} FC, the real and imaginary part of fundamental FC of n^{th} DAB state variables i_{Lsn}, v_o and v_{dcn} can be found as,

$$\begin{aligned}\frac{d}{dt}\langle i_{Lsn}\rangle_0 = \; & -\frac{R_{sn}}{L_{sn}}\langle i_{Lsn}\rangle_0 + \frac{1}{L_{sn}}\Big[\langle s_{prin}\rangle_0\langle v_{dcn}\rangle_0 + 2\langle s_{prin}\rangle_1^R\langle v_{dcn}\rangle_1^R + 2\langle s_{prin}\rangle_1^I\langle v_{dcn}\rangle_1^I\Big] \\ & - \frac{1}{L_{sn}}\Big[\langle s_{secnr}\rangle_0\langle v_o\rangle_0 + 2\langle s_{secnr}\rangle_1^R\langle v_o\rangle_1^R + 2\langle s_{secnr}\rangle_1^I\langle v_o\rangle_1^I\Big]\end{aligned} \tag{2.43}$$

$$\frac{d}{dt}\langle i_{Lsn}\rangle_1^R = -\frac{R_{sn}}{L_{sn}}\langle i_{Lsn}\rangle_1^R + \frac{1}{L_{sn}}\Big[\langle s_{prin}\rangle_0\langle v_{dcn}\rangle_1^R + \langle s_{prin}\rangle_1^R\langle v_{dcn}\rangle_0\Big] - \frac{1}{L_{sn}}\Big[\langle s_{secnr}\rangle_0\langle v_o\rangle_1^R + \langle s_{secnr}\rangle_1^R\langle v_o\rangle_0\Big] + \omega\langle i_{Lsn}\rangle_1^I \tag{2.44}$$

$$\frac{d}{dt}\langle i_{Lsn}\rangle_1^I = -\frac{R_{sn}}{L_{sn}}\langle i_{Lsn}\rangle_1^I + \frac{1}{L_{sn}}\Big[\langle s_{prin}\rangle_0\langle v_{dcn}\rangle_1^I + \langle s_{prin}\rangle_1^I\langle v_{dcn}\rangle_0\Big] - \frac{1}{L_{sn}}\Big[\langle s_{secnr}\rangle_0\langle v_o\rangle_1^I + \langle s_{secnr}\rangle_1^I\langle v_o\rangle_0\Big] - \omega\langle i_{Lsn}\rangle_1^R \tag{2.45}$$

$$\frac{d}{dt}\langle v_o\rangle_0 = -\frac{1}{R_oC_o}\langle v_o\rangle_0 + \frac{n}{C_o}\Big[\langle s_{secnr}\rangle_0\langle i_{Lsn}\rangle_0 + 2\langle s_{secnr}\rangle_1^R\langle i_{Lsn}\rangle_1^R + 2\langle s_{secnr}\rangle_1^I\langle i_{Lsn}\rangle_1^I\Big] \tag{2.46}$$

$$\frac{d}{dt}\langle v_{dcn}\rangle_0 = \frac{1}{C_n}\langle i_{dcn}\rangle_0 - \frac{1}{C_n}\Big[\langle s_{prin}\rangle_0\langle i_{Lsn}\rangle_0 + 2\langle s_{prin}\rangle_1^R\langle i_{Lsn}\rangle_1^R + 2\langle s_{prin}\rangle_1^I\langle i_{Lsn}\rangle_1^I\Big] \tag{2.47}$$

The secondary side switching function referred to primary side is denoted by $\big[s_{secnr}(\tau) = N_{tn}s_{secn}(\tau)\big]$. In DAB, the fundamental component of each state variable corresponds to the switching frequency component of that state. The input capacitor (C_n) and output capacitor (C_o) are usually designed so that the switching ripple across the capacitor voltage is less than 1%. As the fundamental switching ripple component in the voltages are negligible, $\langle v_{dcn}\rangle_1^R$, $\langle v_{dcn}\rangle_1^I$, $\langle v_o\rangle_1^R$ and $\langle v_o\rangle_1^I$ can be approximated as zero in the above equations. The FCs of switching function s_{prin} and s_{secn} can be easily derived as,

$$\langle s_{prin}\rangle_0 = 0, \quad \langle s_{prin}\rangle_1^R = 0, \quad \langle s_{prin}\rangle_1^I = -\frac{2}{\pi}, \tag{2.48}$$

$$\langle s_{secn}\rangle_0 = 0, \quad \langle s_{secn}\rangle_1^R = -\frac{2}{\pi}\sin(\pi d_{\varphi n}), \quad \langle s_{secn}\rangle_1^I = -\frac{2}{\pi}\cos(\pi d_{\varphi n}). \tag{2.49}$$

Substituting (2.48), (2.49) and after solving, the dynamic equations can be written in the form of state-space matrix as,

$$\begin{bmatrix} \langle \dot{v}_{dcn} \rangle_0 \\ \langle \dot{v}_o \rangle_0 \\ \langle \dot{i}_{Lsn} \rangle_1^R \\ \langle \dot{i}_{Lsn} \rangle_1^I \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & \frac{4}{\pi C_n} \\ 0 & \frac{-1}{R_o C_o} & \frac{-4nN_{tn}\sin(\pi d_{\varphi n})}{\pi C_o} & \frac{-4nN_{tn}\cos(\pi d_{\varphi n})}{\pi C_o} \\ 0 & \frac{2N_{tn}\sin(\pi d_{\varphi n})}{\pi L_{sn}} & \frac{-R_{sn}}{L_{sn}} & \omega \\ \frac{-2}{\pi L_{sn}} & \frac{2N_{tn}\cos(\pi d_{\varphi n})}{\pi L_{sn}} & -\omega & \frac{-R_{sn}}{L_{sn}} \end{bmatrix} \begin{bmatrix} \langle v_{dcn} \rangle_0 \\ \langle v_o \rangle_0 \\ \langle i_{Lsn} \rangle_1^R \\ \langle i_{Lsn} \rangle_1^I \end{bmatrix} + \begin{bmatrix} \frac{1}{C_n} & 0 & 0 & 0 \end{bmatrix}^T \begin{bmatrix} i_{dcn} \end{bmatrix} \tag{2.50}$$

The state-space matrix in 2.50 represents the large signal dynamic model of DAB using the 0^{th} FC of output voltage, 0^{th} FC the input voltage and 1^{st} FCs of HF-link current.

Linearised Small Signal Model

Designing controllers and analyzing stability for any power converter entails deriving the small signal control-to-output transfer function. This transfer function represents the dynamic response of a converter due to a small perturbation in its control signal. Therefore, from the large signal dynamic model presented in 2.50, a linearised small-signal model is derived by adding a small perturbation to the control input $d_{\varphi n}$. This is given as,

$$\tilde{d}_{\varphi n} = d_{\varphi n} - D_{\varphi n}, \tag{2.51}$$

where, $D_{\varphi n}$ and $\tilde{d}_{\varphi n}$ are the steady state and perturbed control inputs respectively. Perturbation in the control input causes the deviation in the state variables $\langle i_{Lsn} \rangle_1^R$, $\langle i_{Lsn} \rangle_1^I$, $\langle v_o \rangle_0$ and $\langle v_{dcn} \rangle_0$ which are given by,

$$\langle \tilde{i}_{Lsn} \rangle_1^R = \langle i_{Lsn} \rangle_1^R - I_{Lsn1R},$$

$$\langle \tilde{i}_{Lsn} \rangle_1^I = \langle i_{Lsn} \rangle_1^I - I_{Lsn1I},$$

$$\langle \tilde{v}_o \rangle_0 = \langle v_o \rangle_0 - V_o,$$

$$\langle \tilde{v}_{dcn} \rangle_0 = \langle v_{dcn} \rangle_0 - V_{dcn},$$

where, $\langle \tilde{i}_{Lsn} \rangle_1^R$, $\langle \tilde{i}_{Lsn} \rangle_1^I$, $\langle \tilde{v}_o \rangle_0$, $\langle \tilde{v}_{dcn} \rangle_0$ are the perturbed state variables. I_{Lsn1R}, I_{Lsn1I}, V_o, V_{dcn} represents the steady state values. After linearisation the small signal circuit model is derived, which is given in (2.52), where, $N_{sin} = N_{tn}\sin(\pi D_{\varphi n})$ and $N_{cos} = N_{tn}\cos(\pi D_{\varphi n})$.

$$\begin{bmatrix} \langle \dot{\tilde{v}}_{dcn} \rangle_0 \\ \langle \dot{\tilde{v}}_o \rangle_0 \\ \langle \dot{\tilde{i}}_{Lsn} \rangle_1^R \\ \langle \dot{\tilde{i}}_{Lsn} \rangle_1^I \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & \frac{4}{\pi C_n} \\ 0 & \frac{-1}{R_o C_o} & \frac{-4nN_{sin}}{\pi C_o} & \frac{-4nN_{cos}}{\pi C_o} \\ 0 & \frac{2N_{sin}}{\pi L_{sn}} & \frac{-R_{sn}}{L_{sn}} & \omega \\ \frac{-2}{\pi L_{sn}} & \frac{2N_{cos}}{\pi L_{sn}} & -\omega & \frac{-R_{sn}}{L_{sn}} \end{bmatrix} \begin{bmatrix} \langle \tilde{v}_{dcn} \rangle_0 \\ \langle \tilde{v}_o \rangle_0 \\ \langle \tilde{i}_{Lsn} \rangle_1^R \\ \langle \tilde{i}_{Lsn} \rangle_1^I \end{bmatrix} + \begin{bmatrix} 0 \\ \frac{4n}{C_o}\left[N_{sin} I_{Lsn1I} - N_{cos} I_{Lsn1R}\right] \\ \frac{2N_{cos} V_o}{L_{sn}} \\ -\frac{2N_{sin} V_o}{L_{sn}} \end{bmatrix} \tilde{d}_{\varphi n} \tag{2.52}$$

The input DC-link voltage (v_{dcn}) is usually stiffly regulated by the FEC control in a SST. The input DC-link capacitor (C_n) size is also bulky to suppress the second harmonic ripple. Due to these reasons, v_{dcn} can be ignored as a state variable of the system. From the small signal model given in 2.52 the required transfer functions $G_{vo,d\varphi}$, $G_{iLs1R,d\varphi}$ and $G_{iLs1I,d\varphi}$ can be derived as,

$$G_{vo,d\varphi} = \frac{\langle \tilde{v}_o \rangle_0}{\tilde{d}_\varphi} = \frac{\begin{array}{c} 4N_t(-I_{LS1R}((s^2+\omega^2)L_s^2 + 2L_s R_s s + R_s^2)\pi cos(\pi D_\varphi) \\ + I_{LS1I}((s^2+\omega^2)L_s^2 + 2L_s R_s s + R_s^2)\pi sin(\pi D_\varphi) + (2L_s N_t V_o \omega))R_o \pi \end{array}}{((sC_o R_o + 1)((s^2+\omega^2)L_s^2 + 2L_s R_s s + R_s^2)\pi^2 + (8N_t^2 R_o(sL_s + R_s)))} \tag{2.53}$$

$$G_{iLs1R,d\varphi} = \frac{\langle \tilde{i}_{Ls} \rangle_1^R}{\tilde{d}_\varphi} = \frac{\begin{array}{r} 2N_t(-4((I_{LS1I}s + I_{LS1R}\omega)L_s + I_{LS1I}R_s)N_tR_o\pi cos(\pi D_\varphi)^2 + (-4N_tR_o((-I_{LS1I}\omega + \\ I_{LS1R}s)L_s + I_{LS1R}R_s)\pi sin(\pi D_\varphi) + ((L_ss + R_s)(C_oR_os + 1)\pi^2 + 8N_t^2R_o)V_o) \\ cos(\pi D_\varphi) + 4\pi(-\omega L_s\pi V_o(C_oR_os + 1)sin(\pi D_\varphi)/4 + I_{LS1I}N_tR_o(L_ss + R_s))) \end{array}}{((C_oR_os + 1)((s^2 + \omega^2)L_s^2 + 2L_sR_ss + R_s^2)\pi^2 + 8N_t^2R_o(L_ss + R_s))} \tag{2.54}$$

$$G_{iLs1I,d\varphi} = \frac{\langle \tilde{i}_{Ls} \rangle_1^I}{\tilde{d}_\varphi} = \frac{\begin{array}{r} -2N_t(4N_tR_o((-I_{LS1I}\omega + I_{LS1R}s)L_s + I_{LS1R}R_s)\pi cos(\pi D_\varphi)^2 - 4(((I_{LS1I}s + \\ I_{LS1R}\omega)L_s + I_{LS1I}R_s)N_tR_osin(\pi D_\varphi) - \omega L_s\pi V_o(C_oR_os + 1)/4)\pi cos(\pi D_\varphi) + \\ ((L_ss + R_s)(C_oR_os + 1)\pi^2 + 8N_t^2R_o)V_osin(\pi D_\varphi) + 4I_{LS1I}L_sN_t\pi R_o\omega) \end{array}}{((C_oR_os + 1)((s^2 + \omega^2)L_s^2 + 2L_sR_ss + R_s^2)\pi^2 + 8N_t^2R_o(L_ss + R_s))} \tag{2.55}$$

Using the above transfer functions, controller can be designed for each DAB module in the modular SST, to meet the desired control objective.

2.4 Validation Through Simulation

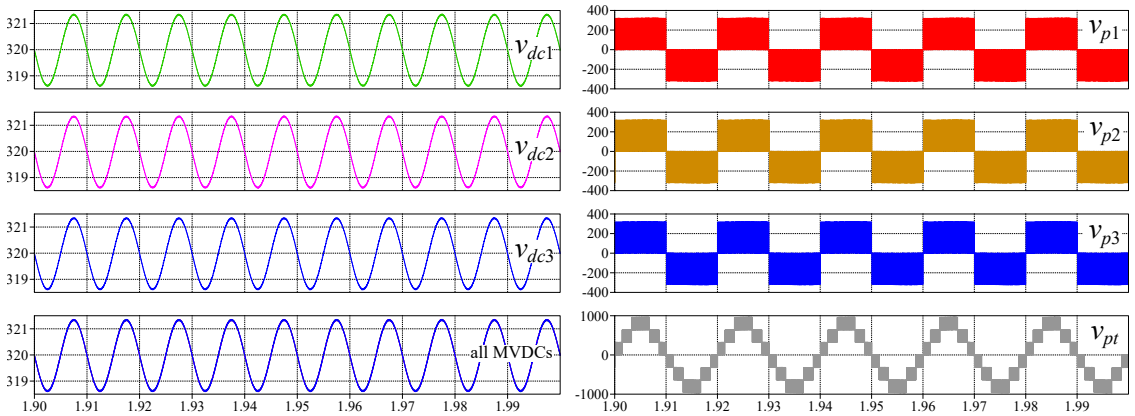
The impact of equal and unequal modulation duty cycles on the THD of grid current is analysed through simulation for the CMFEC. Additionally, the validation of GA model for the OPDAB is also studied through simulations.

2.4.1 Simulation Results for CMFEC

Table 2.1: Simulation Parameters with 3 cells.

n	$V_{g,RMS}$	V_{dcn}	L_g	C_n	R_{on}	P_n	f_{FEC}
3	540 V	320 V	3.5 mH	4.4 mF	85 Ω	1200 W	4 kHz

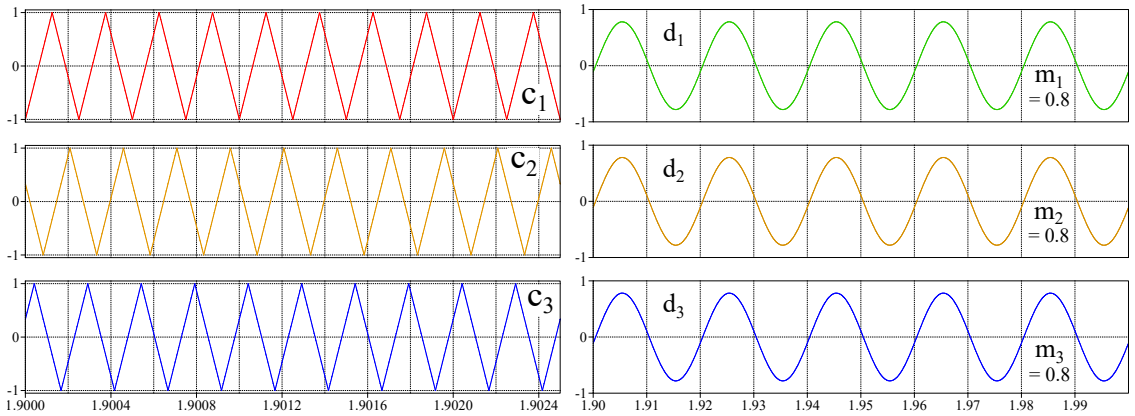
Simulation was performed using PLECS software for the validation. A CMFEC with 3 cells in series was considered. Initially, a case study was considered where all three FECs were connected to the same load resistance (R_{o1} = R_{o2} = R_{o3} = 85 Ω). The simulation parameters are given in Table 2.1. Fig. 2.9a shows that the three MVDCs are balanced and equal to 320V at steady state. The v_{p1}, v_{p2} and v_{p3} voltages are of 3-level due to unipolar



(a) Balanced MVDC link voltages.
X- axis: voltage (volts), Y-axis: time (sec).

(b) Pole voltages.
X- axis: voltage (volts), Y-axis: time (sec).

Figure 2.9: Simulation results showing balanced MVDCs and the pole voltages with same load connected to each FEC module output ($R_{o1} = R_{o2} = R_{o3}$).

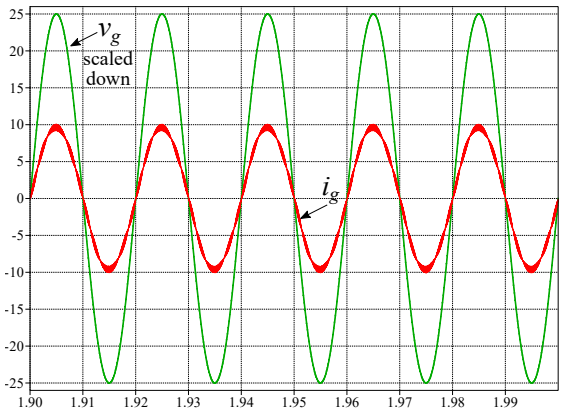


(a) Phase shifted carriers in FECs.
X- axis: voltage (volts), Y-axis: time (sec).

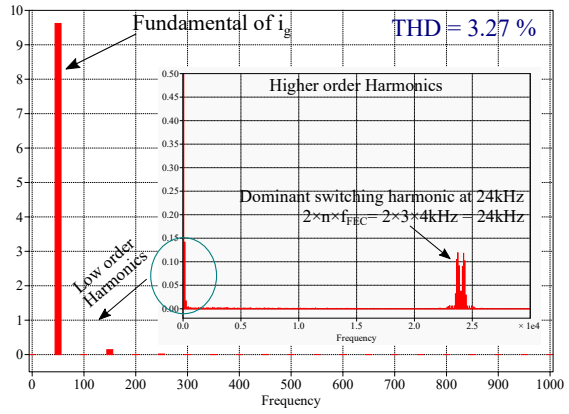
(b) Modulation duty cycle in FECs.
X- axis: voltage (volts), Y-axis: time (sec).

Figure 2.10: Simulation results showing phase shifted carriers and individual modulation duty cycles with same load connected to each FEC module output ($R_{o1} = R_{o2} = R_{o3}$).

PWM as shown in Fig. 2.9b. The total pole voltage v_{pt} is of $(2 \times 3 + 1) = 7$ levels. It is because the carrier signals are interleaved with phase shift angle of $360^0/3 = 120^0$ as shown in Fig. 2.10a. The three modulation duty cycles d_1, d_2 and d_3 are same, with each having modulation index of 0.8 as shown in Fig. 2.10b. These duty cycles are identical because of the equal power transfer in each FEC module. The grid current i_g in UPF operation is shown in Fig. 2.11a. The dominant higher order switching harmonics were

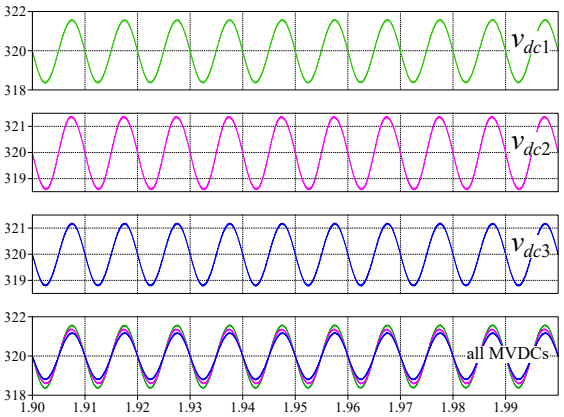


(a) Grid voltage and grid current.
$v_g \rightarrow$ X- axis: voltage (volts), Y-axis: time (sec).
$i_g \rightarrow$ X- axis: current (Amp), Y-axis: time (sec).

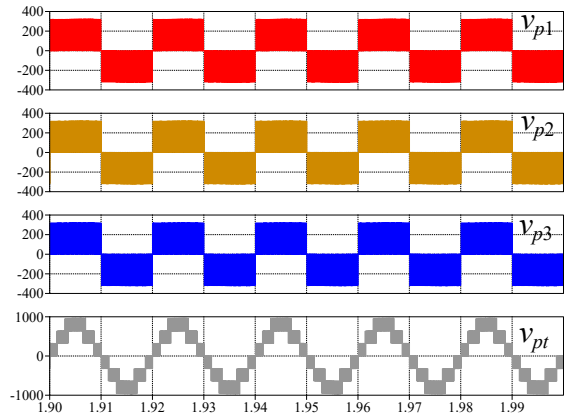


(b) FFT plot of grid current i_g.
X- axis: current (Amp), Y-axis: frequency (Hz).

Figure 2.11: Simulation result showing grid side UPF operation and FFT plot of current drawn from grid with same load connected to each FEC module output ($R_{o1} = R_{o2} = R_{o3}$).



(a) Balanced MVDC link voltages.
X- axis: voltage (volts), Y-axis: time (sec).

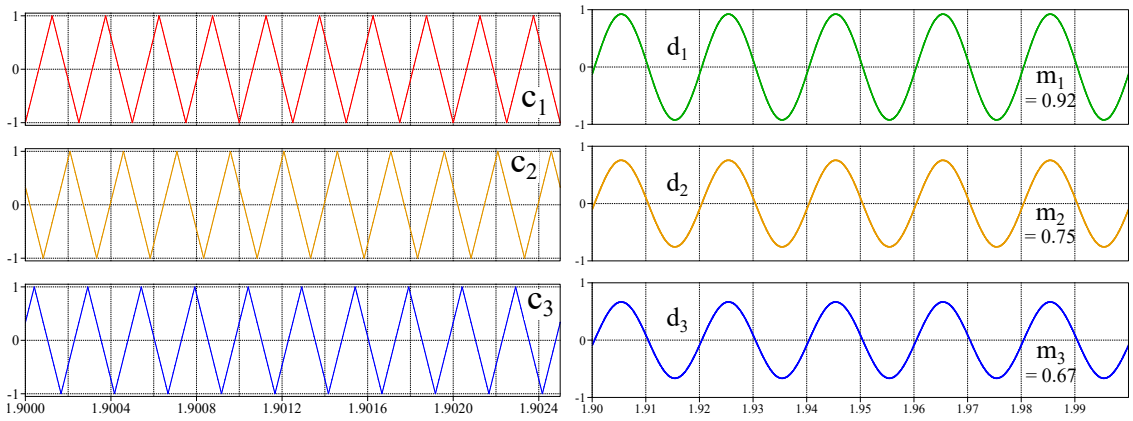


(b) Pole voltages.
X- axis: voltage (volts), Y-axis: time (sec)..

Figure 2.12: Simulation results showing balanced MVDCs and the pole voltages with 15% variation in load connected to each FEC module output ($R_{o1} \neq R_{o2} \neq R_{o3}$).

observed to be centered around ($2 \times 3 \times 4$ kHz = 24 kHz) as shown in Fig. 2.11b. The THD of grid current was found to be 3.27% under this equal load power sharing condition.

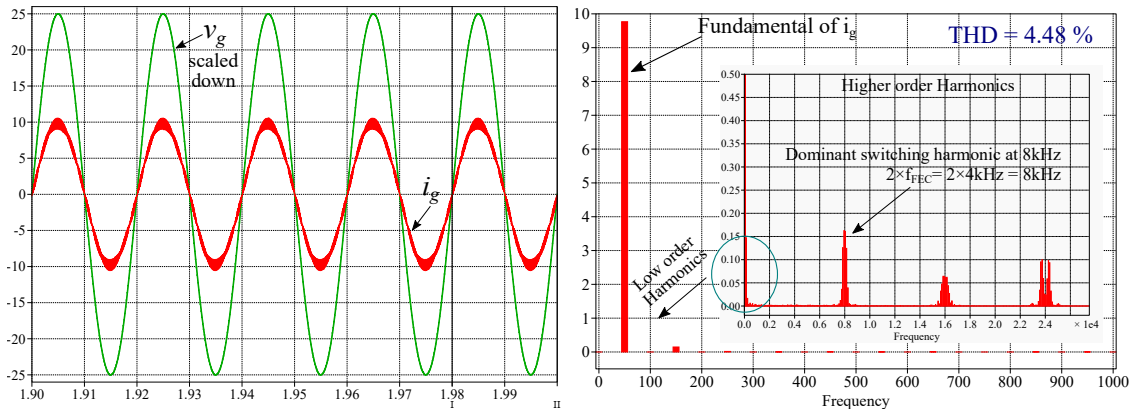
In the next series of simulations, a load power variation of $\pm 15\%$ was taken into account. The load resistance values of three FECs are selected as $R_{o1} = 72\Omega$, $R_{o2} = 85\Omega$, $R_{o3} = 98\Omega$. The MVDC voltages are maintained at 320V and the pole voltage (v_{pt}) have



(a) Phase shifted carriers in FECs.
X- axis: voltage (volts), Y-axis: time (sec).

(b) Modulation duty cycle in FECs.
X- axis: voltage (volts), Y-axis: time (sec).

Figure 2.13: Simulation results showing phase shifted carriers and individual modulation duty cycles with 15% variation in load connected to each FEC module output ($R_{o1} \neq R_{o2} \neq R_{o3}$).



(a) Grid voltage and grid current.
$v_g \rightarrow$ X- axis: voltage (volts), Y-axis: time (sec).
$i_g \rightarrow$ X- axis: current (Amp), Y-axis: time (sec).

(b) FFT plot of grid current i_g.
X- axis: current (Amp), Y-axis: frequency (Hz).

Figure 2.14: Simulation result showing grid side UPF operation and FFT plot of current drawn from grid with 15% variation in load connected to each FEC module output ($R_{o1} \neq R_{o2} \neq R_{o3}$).

7 levels, as illustrated in Figure 2.12. It can be noticed that, due to differences in power transfer, the second harmonic ripple in the MVDCs are unequal. The modulation duty cycles are non-identical because of load power imbalance, with modulation index $m_1 = 0.92$, $m_2 = 0.75$ and $m_3 = 0.67$. This is depicted in Fig. 2.13. The grid current and its FFT

plot is shown in Fig. 2.14. Notably, the lowest dominant switching harmonics are centered around 8kHz instead of 24kHz, leading to a higher THD of 4.48% in the grid current.

These simulation results highlight that unequal modulation duty cycles in the CMFEC stage, attributed to power imbalances, can result in higher grid current distortion. This provides another motivation to achieve equal voltage and power distribution within a modular SST during steady-state. In SST, DAB converter behaves as an load to each FEC. The mismatch in DAB HF-link inductance and turns ratio can cause imbalance in power transfer, eventually causing more grid current distortion. It is essential to have a precise current control for ensuring equal power sharing among the SST cells.

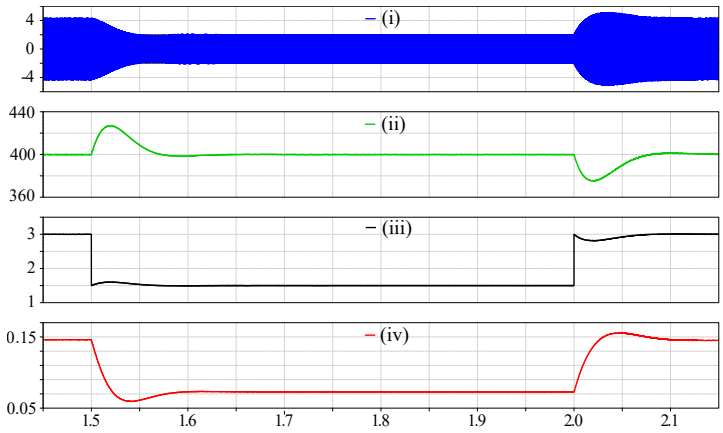
2.4.2 Simulation Results for OPDAB

Table 2.2: Simulation Parameters

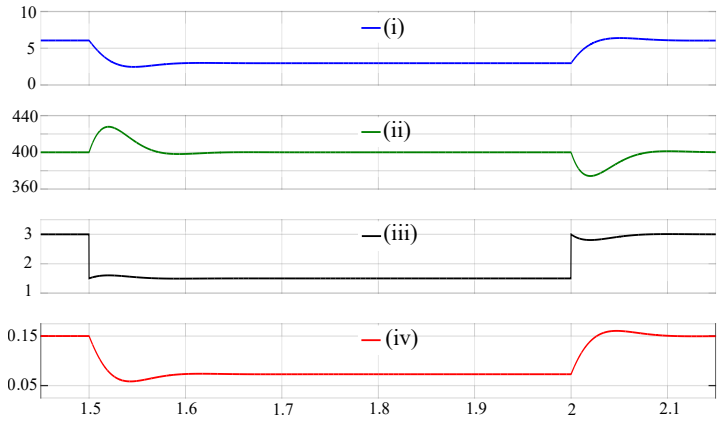
L_g	L_{sn}	R_{sn}	C_{dcn}	C_o	f_{DAB}	f_{FEC}	N_{tn}	V_{dcn}	V_o	V_g	P_n
15mH	250μH	0.02Ω	2200μF	470μF	20kHz	4kHz	4:5	320V	400V	190V	1.2kW

The generalized average (GA) model of the DAB circuit was simulated using MATLAB. Subsequently, the actual DAB circuit was simulated using PLECS for the purpose of comparison. The parameter values used for simulation are provided in Table 2.2. Two different load change conditions were applied as disturbances sequentially: a step decrease in load from full load to half load at 1.5 seconds, and a step increase in load from half load to full load at 2 seconds. These disturbances were used to analyse and compare the dynamic behaviour, as illustrated in Fig. 2.15. The transient characteristics, such as the peak overshoot approximately $\pm 6.75\%$ and settling time of 60 ms, were found to be nearly identical in both simulations. These results indicate a close match between the mathematical GA model and the circuit simulation.

One of the significant features of this developed model is its ability to capture the dynamic behaviour of the fundamental component of HF-link inductor current ($\langle i_{Lsn} \rangle_1$) en-



(a) DAB Circuit simulation using PLECS

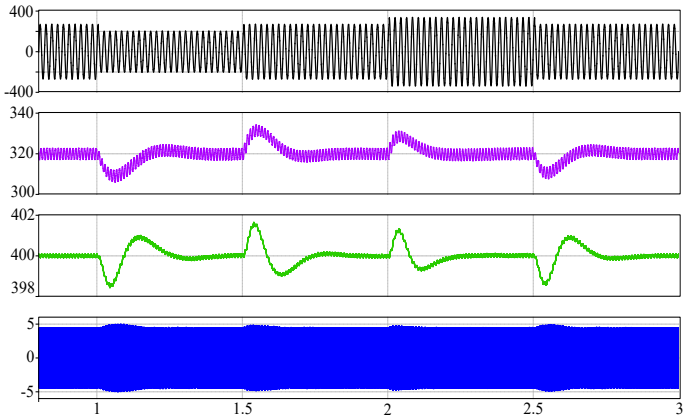


(b) DAB full order GA model simulation using MATLAB

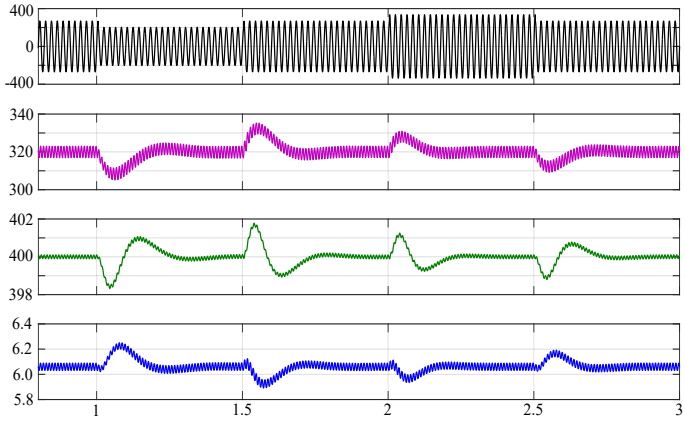
Figure 2.15: Simulation results (a) With PLECS. Top trace: i_{Ls1}, 2nd trace: v_o, 3rd trace: i_o, bottom trace: $d_{\varphi 1}$. (b) With MATLAB. Top trace: $\langle i_{Ls1} \rangle_1$, 2nd trace: v_o, 3rd trace: i_o, bottom trace: $d_{\varphi 1}$. (c) Top trace: i_{Ls1} with PLECS, Bottom trace: $\langle i_{Ls1} \rangle_1$ with MATLAB.

velope, which is predominantly responsible for the power transfer. It can be calculated by $\langle i_{Lsn} \rangle_1 = 2\sqrt{(\langle i_{Lsn} \rangle_1^R)^2 + (\langle i_{Lsn} \rangle_1^I)^2}$. In contrast, the reduced-order model fails to provide any insights into the dynamic behaviour of HF-link current. The $\langle i_{Lsn} \rangle_1$ information obtained from this developed GA model closely resembles the envelope of the HF-link current. It can serve as a reliable indicator for predicting the saturation of the HF-link magnetics core, when the operating flux density exceeds the saturation flux density.

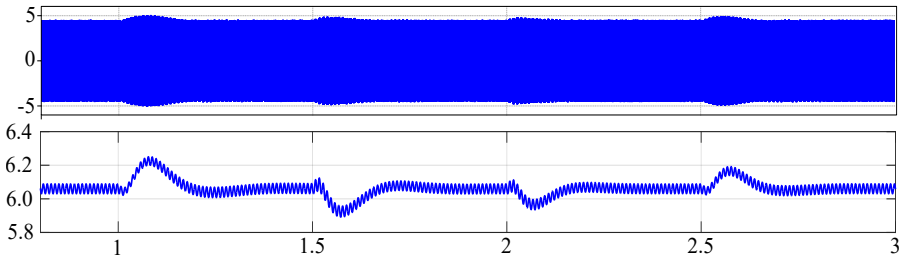
A grid voltage disturbance was introduced into the system, consisting of a 25% sag from 1.005 seconds to 1.505 seconds, followed by a 25% swell from 2.005 seconds to 2.505



(a) FEC-DAB combination circuit simulation using PLECS



(b) FEC-DAB combination GA model simulation with MATLAB



(c) DAB Inductor current comparison (for grid voltage sag and swell)

Figure 2.16: Simulation results (a) With PLECS. Top trace: v_g, 2nd trace: v_{dc1}, 3rd trace: v_o, bottom trace: i_{Ls1}. (b) With MATLAB. Top trace: v_g, 2nd trace: v_{dc1}, 3rd trace: v_o, bottom trace: $\langle i_{Ls1} \rangle_1$. (c) Top trace: i_{Ls1} with PLECS, Bottom trace: $\langle i_{Ls1} \rangle_1$ with MATLAB.

seconds. This disturbance was applied at the peak of the grid voltage and the dynamic behaviour of a single-cell FEC-DAB combination was analysed, as shown in Fig. 2.16. The transient properties observed include the peak overshoot in the MVDC link voltage

(v_{dc1}) and the output LVDC link voltage (v_o), which are approximately within $\pm 4.5\%$ and $\pm 0.375\%$ respectively, for both grid voltage sag and swell conditions. The settling time is close to 85ms for v_{dc1}. The FEC side control is designed to ensure the rejection of these grid voltage disturbances. Consequently, there is very small variation in both MVDC and LVDC voltages. The variation in the HF-link inductor current is also minimal in response to the 25% sag and swell in grid voltage. The acquired $\langle i_{Lsn} \rangle_1$ from the developed GA model closely resembles the envelope of HF-link current. The above simulation results suggests that the developed model effectively captures the dynamic behaviour of the system under the line and load disturbance transients.

2.5 Concluding Remarks

In this chapter, the low frequency dynamic model development process of SST is addressed. The relevant transfer functions are derived from the small signal model of CMFEC. The modulation scheme of CMFEC is discussed. It was observed from the simulation results that the grid current THD is higher due to unequal modulation duty cycle in CMFEC stage originated from cell-to-cell power imbalance. If the power is balanced it was noted that the dominant higher order harmonic gets shifted to $2nf_{FEC}$ from $2f_{FEC}$ resulting in better grid current quality. Finally, the reduced order model and GA model approach is discussed for the DAB stage. The GA model facilitates capturing the dynamics of HF-link fundamental current envelope, which the reduced order model fails to provide. Consequently, it contributes to enhancing the understanding of the existing system, offering more meaningful insights for design considerations.

Chapter 3

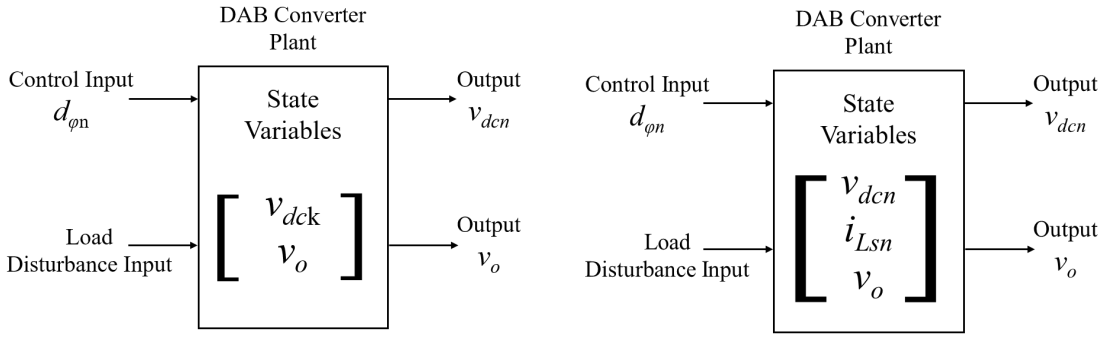
Envelope Tracking Based Control of DAB

The dual loop control, consisting of an outer voltage loop and an inner current loop, is widely regarded as one of the most preferred control technique for any DC-DC or DC-AC converter due to its current limiting capability. When it comes to a DAB converter, effective current control becomes even more critical and essential. This is mainly due to the converter housing a high-frequency transformer, which can enter into saturation due to overcurrent, ultimately resulting in operational failure. Therefore, having information about the HF-link transformer current is crucial for implementing the dual loop control and subsequently preventing the transformer from entering saturation due to overcurrent. Acquiring this information by measuring the HF-link current requires a high-bandwidth (HBW) current sensor and the post sensing signal processing requires a high sampling frequency ADC. This solution is not cost effective and additionally the current sensor requires its own dedicated mounting space as detailed in Chapter 1. Consequently, opting for current sensorless control leads to a more cost effective and compact solution. Therefore, as noted earlier, the central theme of this work is to implement dual loop control through fundamental current estimation without using HBW current sensor. The primary objective is not only to achieve precise current control but also to safeguard the transformer from overcurrent, by regulating its fundamental component and peak envelope in an average sense, without directly measuring it. This unified approach allows both objectives to be addressed

through a centralized current sensorless control structure. This chapter starts with a brief overview of reported schemes and then details the proposed control strategy.

3.1 Reported Control Schemes and the Proposed Strategy

A sensorless power balance control method is introduced in [48], for the DAB stage of modular SST. This approach is based on state space conventional modeling technique, which fails to capture the dynamics of the purely AC HF-link current as its average over a switching period is zero. Sensorless control for DAB is proposed in [57] and [58], where a nonlinear disturbance observer is utilized to estimate the load current. Another approach presented in [59] involves predictive control employing an extended state observer to optimize power transfer by estimation of load current. It's worth noting that none of these approaches incorporate the dynamics of HF-link current in their system dynamic model as they are derived using reduced order model. The reduced order state space model only considers the input and output capacitor voltage as state variable, neglecting the dynamics of HF-link inductor current. The block diagram illustrated in Fig. 3.1 shows that the GA model includes the HF-link current(i_{Lsn}) as a state variable, in contrast to the reduced-order model. This makes the GA model a technically more accurate choice.



(a) Reduced order model **(b)** GA model

Figure 3.1: Block diagram highlighting difference between reduced order and GA model.

A linear observer is employed for the decoupled power control in [38], by estimating HF-link current and segregating its active and reactive component. However, this approach requires measurement of HF-link current using HBW sensor. A reduced order observer to estimate the direct and quadrature component of HF-link current is proposed in [39] for decoupled control. However, this approach relies on measurement of terminal DC link current using HBW sensor. Moreover, the accuracy of estimation during buck mode and boost mode of operation is also noted to be less [60]. A sensorless approach to estimate load current using a proportional-integral observer is introduced in [60]. However, there is a lack of analytical validation results pertaining to HF-link current control.

This work proposes a dual-loop control approach for DAB converter by estimating the HF-link current fundamental component, achieved through the design of a state observer based on GA modeling. Table 4.1 highlights a comparison of various current control strategies, considering the placement of current sensor and the control of HF-link current.

Table 3.1: Comparison of control schemes.

Reference	Sensor Placement	Control of HF-link fundamental current
Ref [47]	Yes (HF AC link)	Yes
Ref [34]	Yes (HF AC link)	Yes
Ref [36]	Yes (HF AC link)	Yes
Ref [38]	Yes (HF AC link)	No
Ref [39]	Yes (Terminal DC link)	No
Ref [48]	No	No
Ref [57]	No	No
Ref [58]	No	No
Ref [59]	No	No
Ref [60]	No	No
Proposed	No	Yes

The key features of this proposed control scheme are,

1. Eliminating the necessity of HBW current sensor and high sampling frequency.
2. Providing current control capability with direct control handle on HF-link fundamental component.
3. Enabling online real-time monitoring of the peak envelope of HF-link current and seamlessly integrating it into the inner current loop. This serves to pre-emptively prevent the saturation of the magnetic core in the HF-link due to overcurrent.

In the subsequent sections of this chapter, the proposed HBW current sensorless control strategy, the full order state observer design to estimate the fundamental component and monitor the peak envelope is discussed sequentially. Finally relevant experimental results are provided for validation.

3.2 Current Envelope Estimation Based Control

The proposed current sensorless dual loop control of DAB converter is based on the estimation using full order state observer. The block diagram of the proposed control strategy

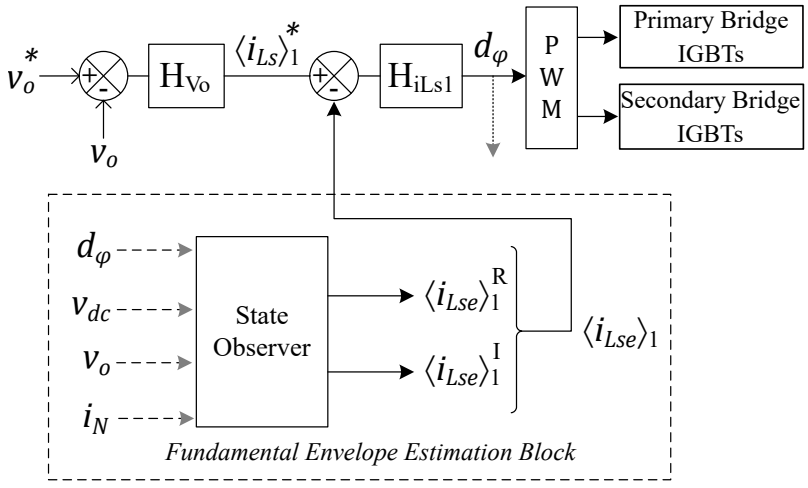


Figure 3.2: Control scheme for dual loop control of DAB with HF-link current fundamental envelope estimation using state observer.

is presented in Fig. 3.2. It features an outer control loop for regulating the DC voltage output similar to other reported methods. This method stands out due to its incorporation of an inner loop that governs the fundamental component of HF-link current through an envelope control method. Apart from not relying on a current sensor, this envelope control method offers two other significant benefits. First, the estimated fundamental component alone with the information of v_{dc} and v_o, can serve the purpose of monitoring the peak current envelope of HF-link. Consequently, a real-time online estimation for the peak current becomes possible. It can be easily integrated within the inner loop to prevent saturation of the HF-link magnetic core. The second advantage is that by estimating the envelope of HF-link current instead of directly estimating entire HF-link current, it yields an equally effective control and saturation prevention tool compared to other reported techniques. Besides, estimating only the envelope makes the computational overhead requirement much lesser than estimating the current itself. A full order state observer is employed to estimate this envelope. The observer design procedure is discussed sequentially.

3.2.1 Observer Design

The procedure for designing a full-order state observer is simple. It is developed from the linearised small signal model derived in the previous chapter. The small signal model is again reproduced here and shown in (3.1), where, $\tilde{i}_N$ represents the output load disturbance. The linearised small signal model can be represented as,

$$\dot{\tilde{\mathbf{x}}} = \mathbf{A}\tilde{\mathbf{x}} + \mathbf{B_1}\tilde{d_\varphi} + \mathbf{B_2}\tilde{v}_{dc} + \mathbf{B_3}\tilde{i}_N. \tag{3.2}$$

The observer design based on this model is directly extended to estimate the large signal state variables. The primary assumption is that the transition from one static equilibrium point to another in the large signal model takes place through a series of disturbances or perturbations in the small signal model. The block diagram of the system with state observer

$$\underbrace{\begin{bmatrix} \langle\dot{\tilde{v}}_o\rangle_0 \\ \langle\dot{\tilde{i}}_{Ls}\rangle_1^R \\ \langle\dot{\tilde{i}}_{Ls}\rangle_1^I \end{bmatrix}}_{\dot{\tilde{\mathbf{x}}}} = \underbrace{\begin{bmatrix} \frac{-1}{R_oC_o} & -\frac{4N_{sin}}{\pi C_o} & -\frac{4N_{cos}}{\pi C_o} \\ \frac{2N_{sin}}{\pi L_s} & -\frac{R_s}{L_s} & \omega \\ \frac{2N_{cos}}{\pi L_s} & -\omega & -\frac{R_s}{L_s} \end{bmatrix}}_{\mathbf{A}} \underbrace{\begin{bmatrix} \langle\tilde{v}_o\rangle_0 \\ \langle\tilde{i}_{Ls}\rangle_1^R \\ \langle\tilde{i}_{Ls}\rangle_1^I \end{bmatrix}}_{\tilde{\mathbf{x}}} + \underbrace{\begin{bmatrix} \frac{4}{C_o}\Big[N_{sin}I_{Ls1I} - \\ N_{cos}I_{Ls1R}\Big] \\ \frac{2N_{cos}}{L_s}V_o \\ -\frac{2N_{sin}}{L_s}V_o \end{bmatrix}}_{\mathbf{B_1}} \underbrace{\tilde{d}_\varphi}_{u_1}$$
$$+ \underbrace{\begin{bmatrix} 0 \\ 0 \\ -\frac{2}{\pi L_s} \end{bmatrix}}_{\mathbf{B_2}} \underbrace{\tilde{v}_{dc}}_{u_2} + \underbrace{\begin{bmatrix} -\frac{1}{C_o} \\ 0 \\ 0 \end{bmatrix}}_{\mathbf{B_3}} \underbrace{\tilde{i}_N}_{u_3} \tag{3.1}$$

is illustrated in Fig. 3.3. The equation corresponding to output is shown in (3.3), where only $\langle v_o\rangle_0$ voltage is measured directly using a low band width voltage sensor. Hence, $\mathbf{C} = \begin{bmatrix} 1 & 0 & 0 \end{bmatrix}$.

$$y = \mathbf{C}\mathbf{x} = \begin{bmatrix} 1 & 0 & 0 \end{bmatrix}\mathbf{x} \tag{3.3}$$

One of the initial requirements for this observer design is to determine whether the system is observable or not. The observability matrix ($\mathbf{O_M}$) is given by,

$$\mathbf{O_M} = \begin{bmatrix} \mathbf{C} & \mathbf{CA} & \mathbf{CA}^2 \end{bmatrix}^T. \tag{3.4}$$

The rank of $\mathbf{O_M}$ matrix can be easily calculated and it can be verified that it is of full rank. Hence this confirms that the system is completely observable. Subsequently, a simple conventional pole placement method is applied for the estimation of HF-link current fundamental envelope ($\langle i_{Lse}\rangle_1$). Typically, the poles of the state observer are positioned sufficiently far away from the left half of the s-plane to ensure that the error in estimation

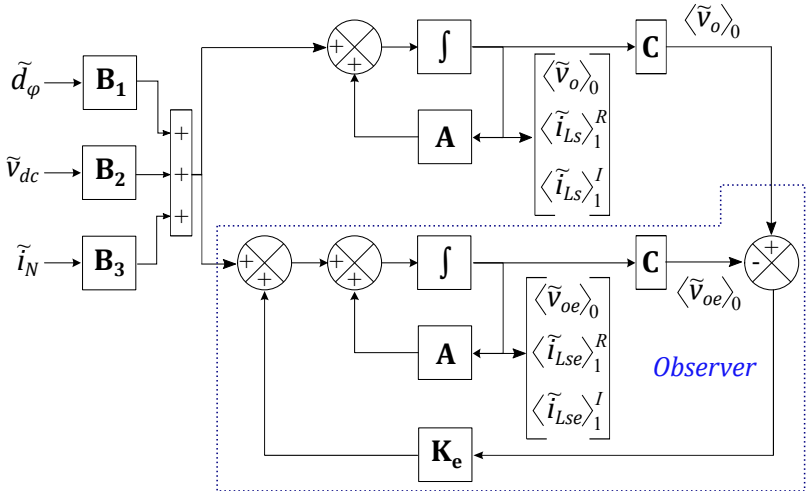


Figure 3.3: Full order state observer for fundamental envelope estimation.

quickly decays to zero. The error dynamics can be represented as,

$$\dot{\mathbf{e}} = \dot{\mathbf{x}} - \dot{\mathbf{x}}_e = (\mathbf{A} - \mathbf{K_e C})\mathbf{e}. \tag{3.5}$$

Here, error $\mathbf{e}$ is the difference between actual state and the estimated state and $\mathbf{x}_e = \begin{bmatrix} \langle v_{oe}\rangle_0 & \langle i_{Lse}\rangle_1^R & \langle i_{Lse}\rangle_1^I \end{bmatrix}^T$, are the estimated state variables. Mathematical model of full order state observer can be obtained as,

$$\dot{\mathbf{x}}_e = (\mathbf{A} - \mathbf{K_e C})\mathbf{x}_e + \mathbf{B_1} d_\varphi + \mathbf{B_2} v_{dc} + \mathbf{B_3} i_N + \mathbf{K_e} v_o, \tag{3.6}$$

where, $\mathbf{K_e}$ is the observer gain matrix and it minimizes the error between actual state and estimated state. $\mathbf{K_e}$ can be derived using Ackermann's formula for observer pole placement, which is given as,

$$\mathbf{K_e} = \phi(\mathbf{A}) \begin{bmatrix} \mathbf{C} \\ \mathbf{CA} \\ \mathbf{CA}^2 \end{bmatrix}^{-1} \begin{bmatrix} 0 \\ 0 \\ 1 \end{bmatrix}. \tag{3.7}$$

Using Cayley–Hamilton's theorem, $\phi(\mathbf{A})$ matrix can be found as,

$$\phi(\mathbf{A}) = \mathbf{A}^2 - 2(OP_1 + OP_2)\mathbf{A} + OP_1OP_2\mathbf{I}, \tag{3.8}$$

where, OP_1 and OP_2 are the desired observer poles and the eigen values of $(\mathbf{A} - \mathbf{K_e C})$ matrix. $\mathbf{I}$ is the identity matrix. During design, these observer poles can be selected five to ten times higher than that of the inner loop controller poles for fast convergence.

After the estimation of $\langle i_{Lse} \rangle_1^R$ and $\langle i_{Lse} \rangle_1^I$ using (3.6), the estimated HF-link current fundamental envelope $\langle i_{Lse} \rangle_1$ can be obtained as,

$$\langle i_{Lse} \rangle_1 = 2\sqrt{(\langle i_{Lse} \rangle_1^R)^2 + (\langle i_{Lse} \rangle_1^I)^2}. \tag{3.9}$$

The estimated output current (i_{oe}) can also be found using,

$$i_{oe} = \frac{4}{\pi}\sqrt{(\langle i_{Lse} \rangle_1^R \sin\varphi)^2 + (\langle i_{Lse} \rangle_1^I \cos\varphi)^2}. \tag{3.10}$$

This observer based dual loop observed-state feedback control can be implemented easily on a digital control platform. Estimating the HF-link current envelope in place of the HF-link current itself enables the placement of observer poles at a much lower frequency than the switching frequency. Hence the required sampling time is less during digital implementation. In this work, the sampling frequency is selected as equal to the switching frequency.

3.2.2 Monitoring of Peak Envelope

To prevent the saturation of HF-link inductor, it is crucial to ensure that the peak operating flux density must remain below the saturation flux density (B_{sat}). This requires the peak current to be lesser than the threshold determined by the B_{sat} of the magnetic material

and the core geometry. It is crucial to ensure that the peak current does not surpass this limit. This gives the primary motivation to track the peak envelope of HF-link current. A maximum current threshold can be set depending on the operating conditions and specific magnetic core being used. Once the estimated peak envelope approaches the predefined maximum threshold current limit, the inner loop reference selector block (RSB) is used to clamp the current reference. This is shown in Fig. 3.4.

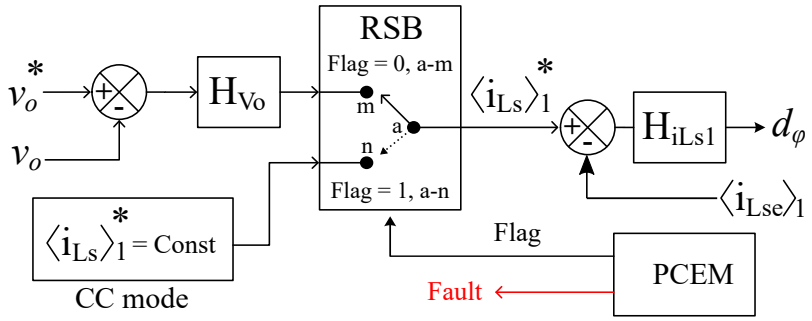


Figure 3.4: Fundamental harmonic control with peak current envelope monitoring.

When the peak current value approaches the preset maximum current threshold, the peak current envelope monitoring (PCEM) block produces a high flag. It simultaneously triggers a fault signal. The DAB converter works in constant voltage (CV) regulation mode, when the flag is set to 0. When this flag goes high, the inner reference $\langle i_{Ls} \rangle_1$ is clamped to a constant value which is same as the previously stored pre-fault value of $\langle i_{Ls} \rangle_1$ just before the transition of flag. The operation of the PCEM block is explained next.

The DAB converter waveforms in one switching cycle is illustrated in Fig. 3.5. i_{LC} and i_{LB} are the peak values of HF-link current i_{Ls}, for the buck and boost modes of operation respectively. i_{LB} and i_{LC} are equal for unity gain mode operation. Based on the waveform and its Fourier series expansion, the following relationships are derived.

$$\langle i_{Ls} \rangle_1^R = \frac{-\pi i_{sum}(1-\cos\varphi)+2\varphi(i_{LB}-i_{LC}\cos\varphi)}{\pi\varphi(\pi-\varphi)}, \tag{3.11}$$

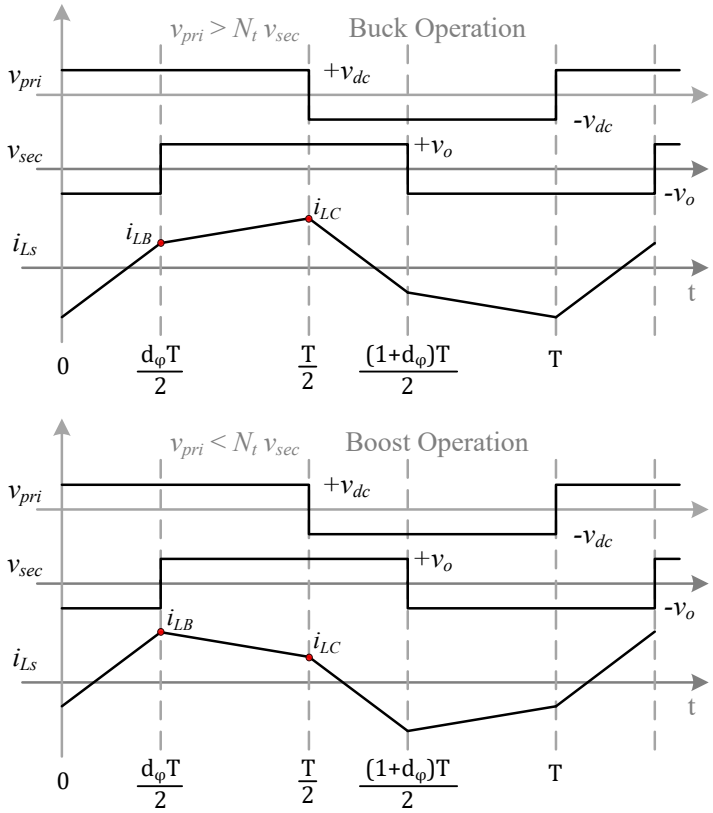


Figure 3.5: DAB waveforms during one switching period.

$$\langle i_{Ls} \rangle_1^I = \frac{-[\pi i_{sum} - 2\varphi i_{LC}] \sin\varphi}{\pi\varphi(\pi - \varphi)}, \tag{3.12}$$

$$i_{LB} = i_{LC} - \big[v_{net}(\pi - \varphi)/X_{Ls}\big], \tag{3.13}$$

where, $i_{sum} = (i_{LB} + i_{LC})$, φ is the phase shift angle between two H-bridges, $X_{Ls} = \omega L_s$ and $v_{net} = v_{dc} - N_t v_o$. Using (3.9), (3.11) to (3.13), i_{LB} and i_{LC} can be estimated as,

$$i_{LCe} = 0.5(\pi - \varphi)\big[v_{net}/X_{Ls}\big] + \frac{\varphi\sqrt{2(\pi X_{Ls}\langle i_{Lse}\rangle_1)^2 - 16(1+\cos\varphi){v_{net}}^2}}{8X_{Ls}\sqrt{(1-\cos\varphi)}}, \tag{3.14}$$

$$i_{LBe} = i_{LCe} - \big[v_{net}(\pi - \varphi)/X_{Ls}\big]. \tag{3.15}$$

To facilitate digital implementation, a simplified and approximate expression of (3.14) and (3.15) is derived next in the per-unit (pu) system. The chosen base values are: base

voltage $V_b = v_{dc}$, base current $I_b = V_b/Z_b$ and base impedance $Z_b = \omega L_s$. The reflected voltage gain is defined as $M_r \triangleq N_t(v_o/v_{dc})$. The approximated normalized peak values can be estimated as,

$$i_{LCeN} \approx \frac{\pi}{2}(1-d_\varphi)(1-M_r) + \frac{\pi\varphi}{8\sin(\varphi/2)}\langle i_{Lse}\rangle_{1N}, \tag{3.16}$$

$$i_{LBeN} = i_{LCeN} - (\pi-\varphi)(1-M_r), \tag{3.17}$$

where $\langle i_{Lse}\rangle_{1N} = \langle i_{Lse}\rangle_1/I_b$. The peak current envelope now can be easily traced depending on the mode of operation, after finding i_{LB} and i_{LC} using (3.16) and (3.17). The working of PCEM block is summarized and shown in the Fig. 3.6.

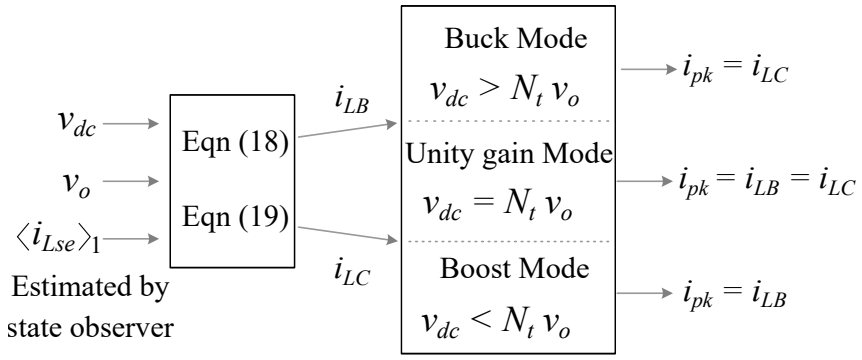
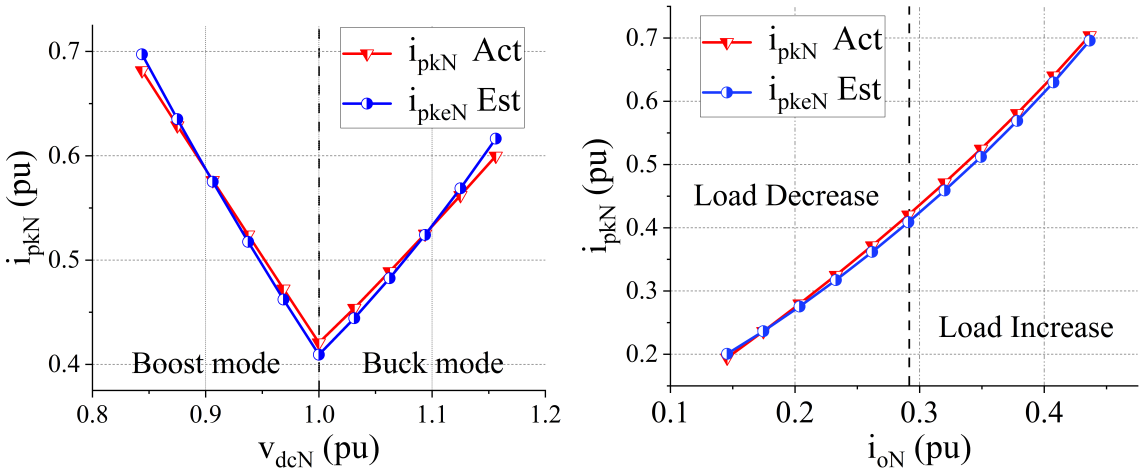


Figure 3.6: Proposed peak current envelope monitoring (PCEM) scheme.

In Figure 3.7, a comparative plot is presented, demonstrating both the actual normalized HF-link current peak (i_{pkN}) obtained through circuit simulation using PLECS and the estimated peak envelope (i_{pkeN}) using (3.16) and (3.17). The comparison is conducted for the rated parameter values considering $\pm 50\%$ load current and $\pm 15\%$ input line voltage variation around their respective nominal values in pu. The percentage error is verified to be less than $\pm 4\%$ for both load and line variations. Therefore, the estimated peak values using (3.16) and (3.17) are used for digital implementation during experimental validations.



(a) Line variation i_o=0.29, v_o=1.25 pu

(b) Load variation v_{dc}=1, v_o=1.25 pu

Figure 3.7: Comparison plot of actual i_{pkN} and estimated i_{pkeN}.

3.3 Correction Factor Inclusion

Circuit diagram of two square wave AC sources separated by a line inductance and phase shifted from each other by phase shift angle φ is shown in Fig. 3.8. Harmonic power transfer between these two sources is,

$$p_{h_n} = \frac{8}{\pi^2}\frac{N_t v_{dc} v_o}{\omega L_s}\sum_{h_n=0}^{\infty}\frac{\sin(2h_n+1)\varphi}{(2h_n+1)^3}, \tag{3.18}$$

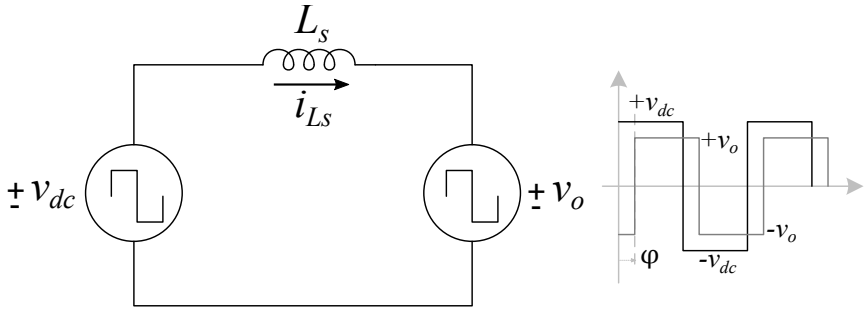


Figure 3.8: Power transfer between two square wave AC sources.

where, the harmonic number is denoted by h_n. The fundamental component of the inductor current ($\langle i_{Ls} \rangle_1$) can be derived as,

$$\langle i_{Ls} \rangle_1 = \frac{\frac{4v_{dc}}{\sqrt{2}\pi}\angle 0 - \frac{4v_o}{\sqrt{2}\pi}\angle \varphi}{\omega L_s \angle 90}. \tag{3.19}$$

The complex power transfer from the input side (s_{fund}) is given by,

$$s_{fund} = p_{fund} + jq_{fund} = \frac{4v_{dc}}{\sqrt{2}\pi}\angle 0 \langle i_{Ls} \rangle_1 \tag{3.20}$$

The active power (p_{fund}) and reactive power (q_{fund}) transfer because of the fundamental component are,

$$p_{fund} = \frac{8}{\pi^2}\frac{N_t v_{dc} v_o}{\omega L_s}\sin\varphi, \tag{3.21}$$

$$q_{fund} = \frac{8}{\pi^2}\frac{v_{dc}}{\omega L_s}\big[v_{dc} - N_t v_o \cos\varphi\big]. \tag{3.22}$$

However, the actual active power transfer in a SPS modulated DAB is,

$$p_{DAB} = \frac{N_t v_{dc} v_o}{\omega L_s}\varphi(1 - \frac{\varphi}{\pi}). \tag{3.23}$$

During GA modelling based on FHA approximation, it is assumed that entire throughput power is transferred due to fundamental component by neglecting the other higher order harmonics. This gives rise to inaccuracy in the earlier developed dynamic model. Therefore, the dynamic model is enhanced by incorporating a correction factor (ε), leading to more accurate estimation. This correction factor can be derived as,

$$\varepsilon = \frac{p_{DAB}}{p_{fund}} = \frac{\pi^2}{8}\frac{\varphi}{\sin\varphi}(1 - \frac{\varphi}{\pi}). \tag{3.24}$$

Following this, all three state variables undergo modification to reconstruct the improved Enhanced FHA (EFHA) model. The detailed derivation is provided in Appendix B.

3.3.1 L_s Identification Scheme

The effectiveness of this proposed control scheme relies on the knowledge of the L_s, its value which may undergo gradual changes over time due to aging. As a result, the accuracy of the estimation can get impacted. To address this issue, an additional L_s parameter identification scheme (PIS) is incorporated. The flowchart of this PIS scheme is depicted in Fig. 3.9. PIS operates each time the system is energised, after which the overall control transits to the proposed method.

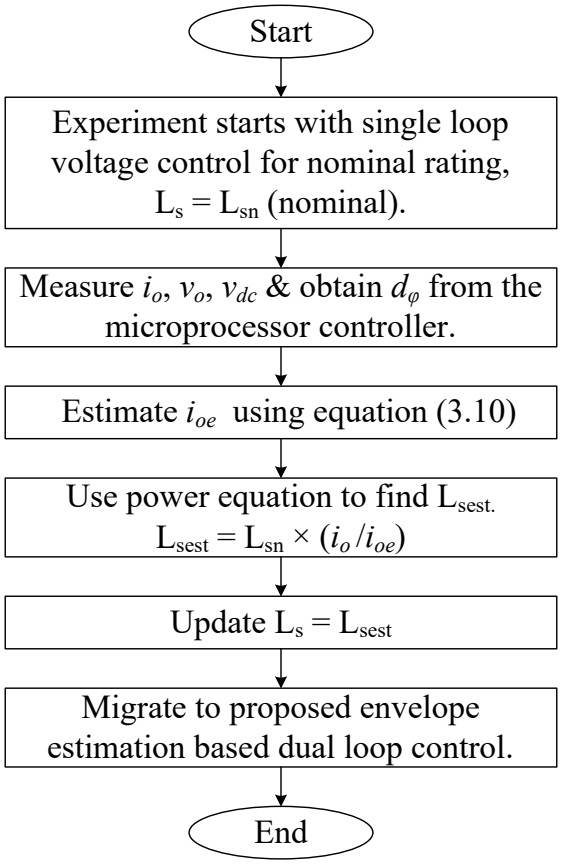


Figure 3.9: Parameter identification scheme (PIS) flowchart.

3.4 Results and Discussion

The initial analysis was conducted through simulations using the PLECS software tool. Experimental validation was carried out using a 650 Watt DAB converter hardware prototype, as illustrated in Fig. 3.10. Discrete IGBTs (IKQ50N120CT2) were employed in both the primary and secondary side H-bridges. The power stage was realized through parallel laminated busbar structure design to minimize stray parasitics. System parameters used during experimental validation are provided in Table. 3.2. Low-cost DSP micro-controller TMS320F28377S was used to realize the complete control logic.

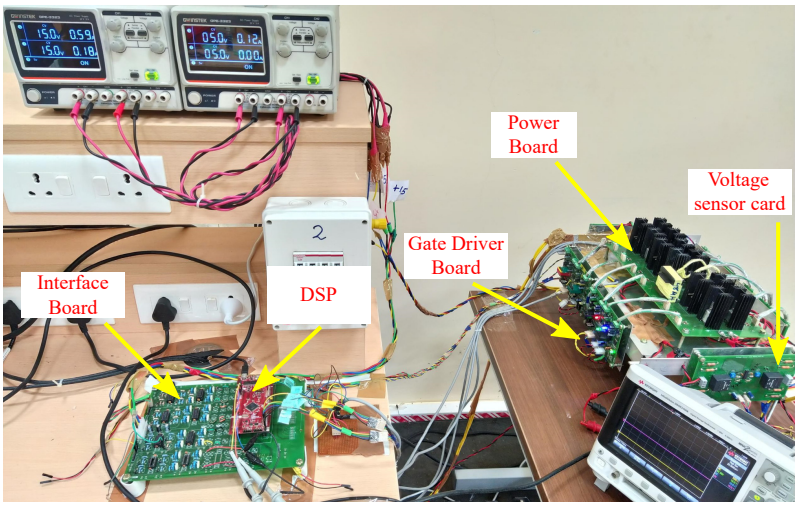


Figure 3.10: Hardware Prototype.

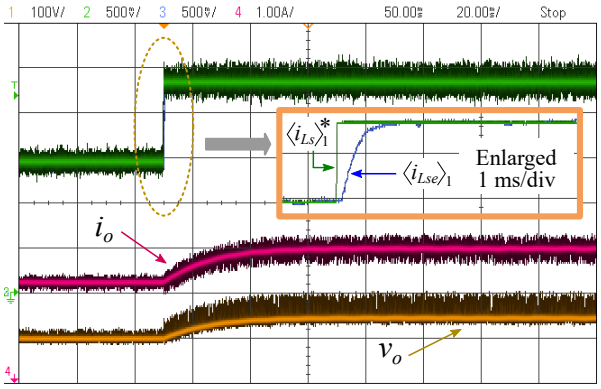
Initially, to assess the ability of the proposed scheme in tracking the fundamental current envelope, the functionality of the inner current loop was investigated. The state observer was used to estimate $\langle i_{Lse} \rangle_1$, serving as the feedback for inner current control loop, as explained earlier. A 40% step increase (2.85 A $\rightarrow$4.8 A) and a 40% step decrease (4.8 A $\rightarrow$2.85 A) in the fundamental current reference ($\langle i_{Ls} \rangle_1^*$) were applied. The corresponding experimental outcomes are illustrated in Fig. 3.11. Both reference $\langle i_{Ls} \rangle_1^*$ and the estimated feedback $\langle i_{Lse} \rangle_1$ waveforms are presented using the 12 bit DACs of micro-controller. The

inner current control loop was designed for bandwidth of 1 kHz. It is evident from Fig. 3.11 that, during both increase and decrease of the reference command, $\langle i_{Lse} \rangle_1$ smoothly tracks $\langle i_{Ls} \rangle_1^*$ without significant overshoot or undershoot. As expected, the settling time was noted to be approximately 0.7 ms. These experimental results demonstrate the current tracking capability of the proposed control scheme.

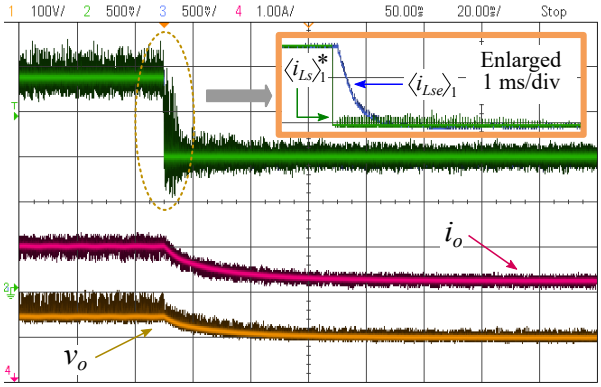
Regulation of the output voltage (v_o) through dual loop control was attempted next. The inner current loop reference $\langle i_{Ls} \rangle_1^*$ was generated by the outer v_o voltage control loop. The estimated $\langle i_{Lse} \rangle_1$ was generated as the feedback from the state observer block. The dynamic performance was evaluated with variation of both output load current and input line voltage. The experimental results associated to 50% step increase in load current (1.625 A $\rightarrow$3.25 A) and 50% step decrease in load current (3.25 A $\rightarrow$1.625 A) are depicted in Fig. 3.12a and Fig. 3.12b respectively. The results presented, including all subsequent experimental results discussed here, were obtained using the EFHA based GA model. The settling time for v_o is nearly 40 ms, whereas, the undershoot/overshoot in v_o is about 7.5% during the step increase and decrease in load respectively.

Table 3.2: System Parameters

Parameter	Symbol	Value
HF link inductance	L_s	114.5 μH
Parasitic Resistance	R_s	1 Ω
Output Capacitance	C_o	550 μF
Switching frequency	f_s	20 kHz
Sampling frequency	f_{samp}	20 kHz
HFT turns ratio	N_t	4:5
Rated input DC voltage	V_{dc}	160 V
Rated output DC voltage	V_o	200 V
Rated power	P	650 W



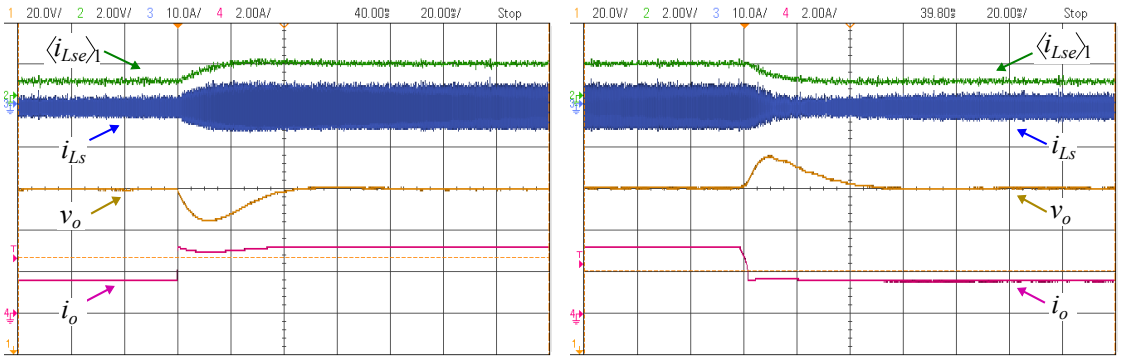
(a) Step increase in $\langle i_{Ls} \rangle_1^*$



(b) Step decrease in $\langle i_{Ls} \rangle_1^*$

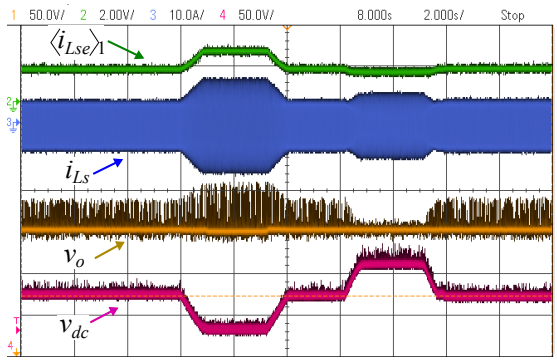
Figure 3.11: Experimental results showing current tracking capability with only inner current loop being functional. Top trace: $\langle i_{Ls} \rangle_1^*$ and $\langle i_{Lse} \rangle_1$ (0.5 V/div), 2nd trace: i_o (1 A/div), Bottom trace: v_o (100 V/div). Normal view - Time 50 ms/div. Enlarged view - Time 1 ms/div.

Upon analysing the data points obtained from the experiments, it was observed that the estimated $\langle i_{Lse} \rangle_1$ very closely matched with the actual $\langle i_{Ls} \rangle_1$ during these load transients. Subsequently, an input voltage disturbance in the form of a ramp with $\pm 15\%$ line variation was introduced, as depicted in Fig. 3.12c. It can be observed that the output voltage v_o remains nearly constant throughout this entire duration. The envelope of i_{Ls} varies in accordance with the changes in v_{dc}. Moreover, it was observed that the estimation accuracy of $\langle i_{Lse} \rangle_1$ was very high. The experimental data collected was plotted in Fig. 3.13 to illustrate the estimation accuracy. Data gathered during experiments with the FHA model were also compiled and are presented here for the purpose of facilitating comparative analysis. From



(a) 50% step increase in load current

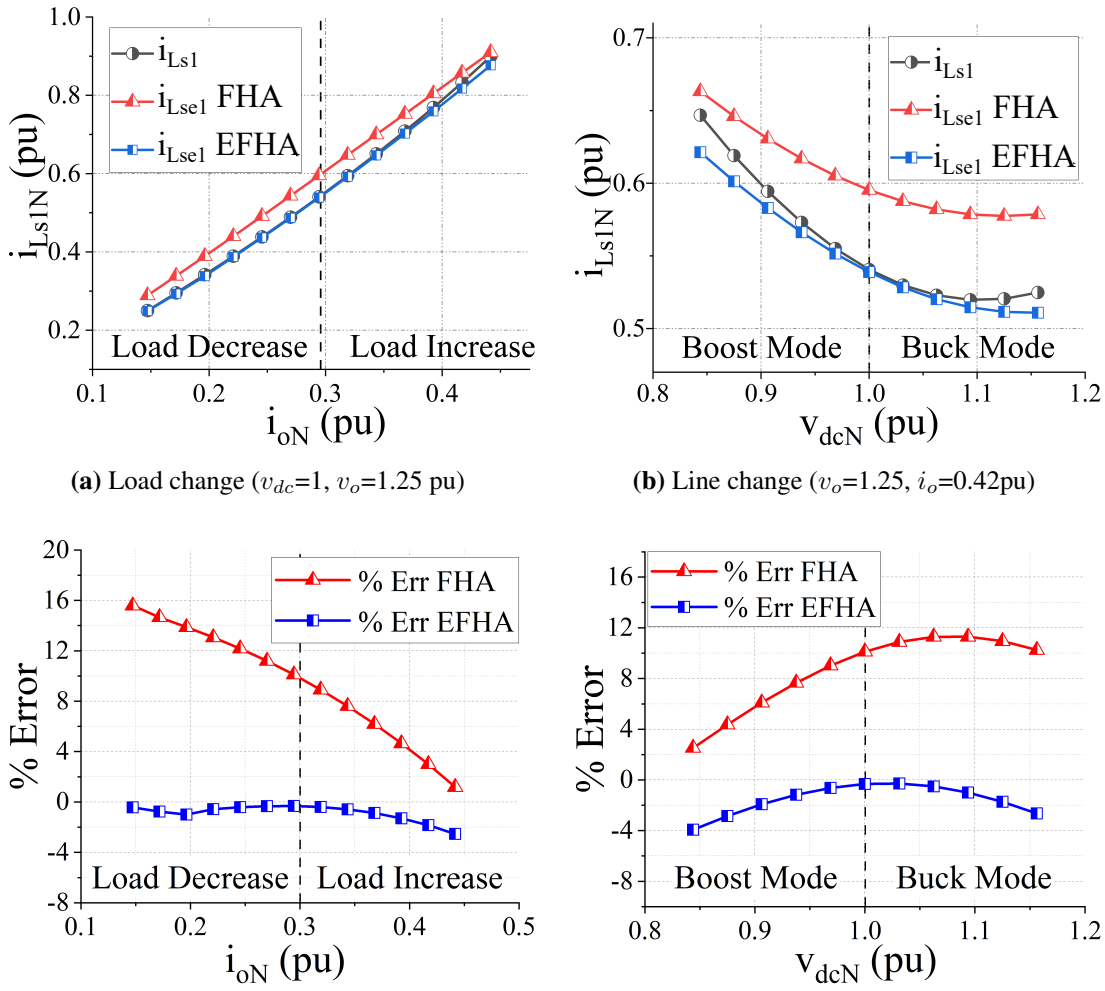
(b) 50% step decrease in load current



(c) 15% ramp variation in input voltage

Figure 3.12: Experimental results for estimation of the fundamental component envelope. Top trace: Estimated $\langle i_{Lse} \rangle_1$ (2 V/div), 2nd trace: i_{Ls} (10 A/div), 3rd trace: v_o (20 V/div), Bottom trace of (a) and (b): i_o (2 A/div), Bottom trace of (c): v_{dc} (50 V/div). (a) and (b): Time 20 ms/div, (c) Time 2 s/div.

the FFT analysis of i_{Ls}, the actual fundamental component $\langle i_{Ls} \rangle_1$ was obtained while regulating the output voltage. The estimated $\langle i_{Lse} \rangle_1$ was acquired from both FHA and EFHA model. The gathered data points were subsequently normalized with respect to the base values and are graphically represented. As expected, it is evident that the EFHA model results in less error. Additionally, it is observed that the accuracy is greater near the operating points where the large signal model is linearized to develop the small signal model. For both a 50% load current variation and a 15% input line voltage variation, $\langle i_{Ls} \rangle_1$ estimation error remains within $\pm 4\%$. Additionally these data also validate the high tracking accuracy for voltage gain other than unity (0.85 to 1.15 in this case).



(a) Load change (v_{dc}=1, v_o=1.25 pu)

(b) Line change (v_o=1.25, i_o=0.42pu)

(c) % error during load variation

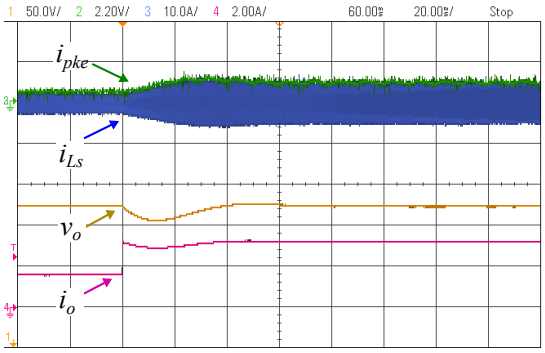
(d) % error during line variation

Figure 3.13: Comparison of experimental $\langle i_{Ls} \rangle_1$ with estimated $\langle i_{Lse} \rangle_1$ from FHA model based observer design and EFHA model based observer design.

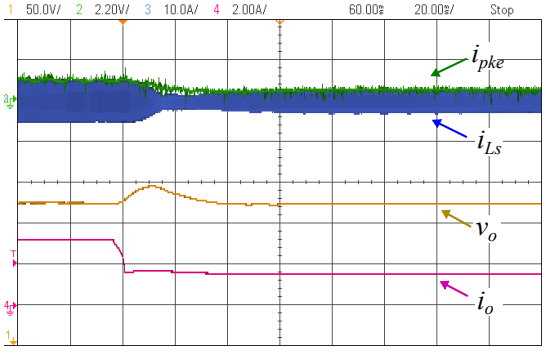
The subsequent series of experiments were conducted to validate the capability of tracking the inductor current peak envelope (i_{pk}). The experimental results corresponding to monitoring of i_{pk} during $\pm$50% step load transients are given in Fig. 3.14a and Fig. 3.14b. It can be clearly observed from the experimental results that the estimated peak envelope (i_{pke}) very closely tracks the actual i_{pk}. Subsequently, a line voltage disturbance was introduced to test the tracking scheme. The experimental result corresponding to this is depicted in Fig. 3.14c. For a $\pm 15\%$ line variation in the v_{dc}, v_o almost remained constant. From the

waveforms, it is clearly evident that envelope i_{pke} tracks actual i_{Ls} with very good accuracy. Analysing the collected data points, it was observed that the estimation accuracy of peak tracking was more than 94% across the entire range of line and load variations. This affirms the effectiveness of the envelope tracking scheme, achieved without the need for any high bandwidth current sensor to measure i_{Ls}.

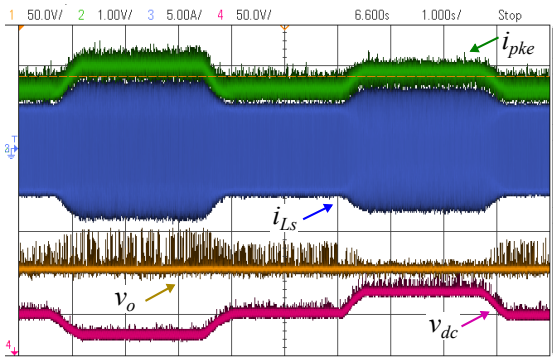
The subsequent experiment aimed to validate the performance of peak current envelope monitoring integrated with the fundamental current control. Experimental results corresponding to this are shown in Fig. 3.15. Based on the magnetic core used in the high frequency transformer, the boundary of inductor peak current (i_{pk}^{B}) corresponding to satu-



(a) 50% step increase in load current

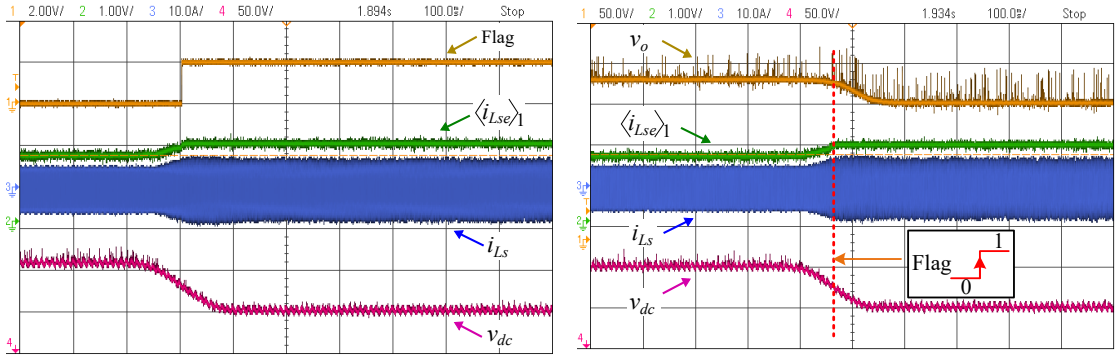


(b) 50% step decrease in load current



(c) 15% ramp variation in input voltage

Figure 3.14: Experimental results for peak envelope estimation. Top trace: Estimated i_{pke} envelope (1 V/div), 2nd trace: Actual i_{Ls} (10 A/div) (a & b), (5 A/div) (c), 3rd trace: v_o (50 V/div), Bottom trace of (a) and (b): i_o (2 A/div), Bottom trace of (c): v_{dc} (50 /div). (a) and (b) Time 20 ms/div, (c) Time 1 s/div.



(a) **(b)**

Figure 3.15: Experimental results showing performance of integrated fundamental current control with peak current envelope monitoring. Top trace of (a): Flag signal (2 V/div), Top trace of (b): v_o (50 V/div). For both (a) and (b): 2nd trace: $\langle i_{Lse} \rangle_1$ (1 V/div), 3rd trace: i_{Ls} (10 A/div), Bottom trace: v_{dc} (50 V/div). Time 100 ms/div.

ration flux density B_{sat} was fixed to 8 A. Subsequently, the input v_{dc} was gradually reduced to run the converter in boost mode. The flag signal generated by PCEM block remains low till the period where i_{pk} is less than i_{pk}^B. The proposed control scheme operates in output voltage regulation mode. Once i_{pk} reaches i_{pk}^B, the flag is raised high. The reference for the inner current control loop $\langle i_{Ls} \rangle_1^*$ automatically gets clamped to a constant value. Hence, the entire control scheme functions in the current regulation/constant current (CC) mode. This constant value of current is a sample of $\langle i_{Ls} \rangle_1$, stored just before the transition of the flag from low to high. This can be observed in Fig. 3.15a. Following this transition to the CC mode, even with a further decrease in v_{dc}, the inductor current fundamental component and the peak envelope remain constant. As a result, v_o is no longer regulated, as evident from Fig. 3.15b. For this transition of the flag from low to high, a fault signal is activated.

Finally, an experiment was conducted to validate the Parameter Identification Scheme (PIS). An operation was conducted assuming the nominal value of L_s as $L_{sn} = 130\mu$H as a case study, while the actual value was $L_{sact} = 114.5\mu$H. The parameters for the state observer were designed based on the value of L_{sn}. The operation commenced with single loop v_o control, as previously illustrated in Fig. 3.9. There is an estimation error of nearly

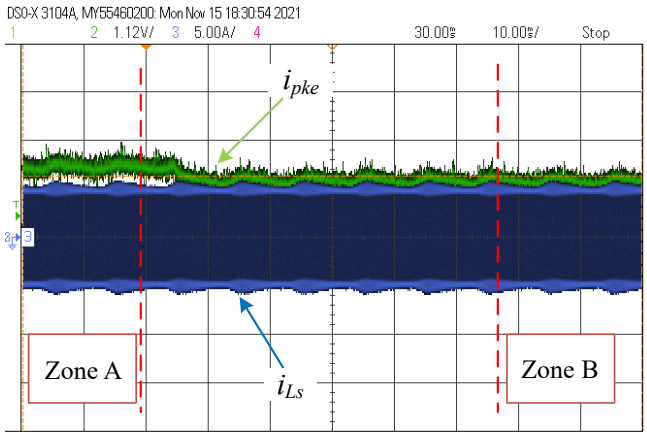


Figure 3.16: Experimental results showing error in i_{pke} estimation due to parametric uncertainty. Top trace: i_{pke} (1.12 V/div), Bottom trace: i_{Ls} (5 A/div). Time 10 ms/div.

7.7% in i_{pke} due to parameter uncertainty, corresponding to the Zone A region in Fig. 3.16. Using (3.10), the output load current i_{oe} is estimated by the state observer designed for L_{sn} = 130 μH. The estimated error of i_o was used to update the value of L_{sn}, resulting in an estimated value of 118μH. The observer coefficients were updated accordingly. Subsequently, it was noticed that the estimation error has decreased to approximately 3.75%. This corresponds to Zone B, where there is a clear reduction in the error in estimating i_{pke}. Since the upper bound for the error in i_{oe} was set to 5%, the final estimation value for L_s was determined to be 118 µH with nearly 97% accuracy. The control scheme then smoothly migrates to the proposed dual-loop control.

Table 3.3: i_{pke} estimation error in zones.

Zone	i_{pk} act (A)	i_{pke} est (A)	% Error in i_{pke}
A	5.2	5.6	7.7%
B	5.2	5.39	3.75%

3.5 Concluding Remarks

In this chapter a dual-loop control for single cell DAB converter based on current envelope estimation is discussed. The key contributions and distinctive characteristics of this work are summarized. The control variable of the inner loop is the fundamental component of inductor current, which is estimated and given as feedback to the inner loop. The online monitoring of peak envelope is performed using this estimated fundamental component. Accurate estimation of the DAB inductance is also implemented to mitigate the impact of parametric variations. Neither the inductor current nor the HF terminal DC link current were measured throughout the process. Hence there was no requirement of high bandwidth current sensor/shunt resistor or high-sampling frequency for the implementation of proposed control scheme. All of these above features were validated through experiments.

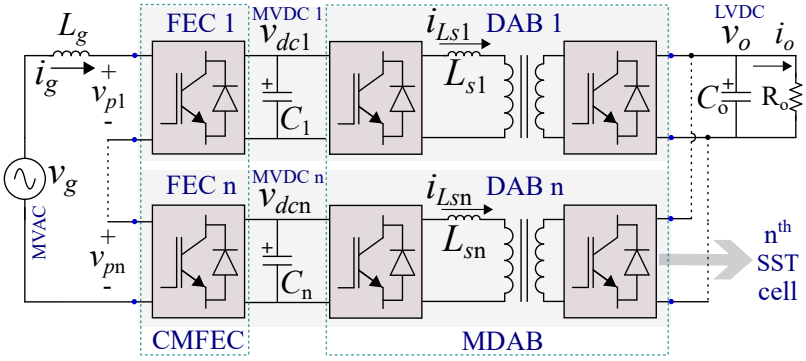
Chapter 4

Estimation Based Flexible Power Sharing Control of ISOP SST

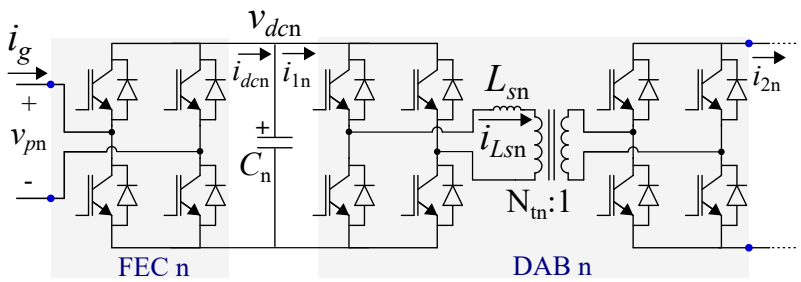
In this chapter, the voltage balance and flexible power sharing control strategy for the modular Input-Series-Output-Parallel (ISOP) configuration is detailed. The high bandwidth (HBW) current sensorless control for a single-cell Dual Active Bridge (DAB), based on HF-link fundamental current envelope estimation, is outlined in Chapter 3. Building upon the foundation established in Chapter 3, a sensorless flexible power sharing control strategy is devised in this chapter, for the 1-phase modular ISOP solid state transformer (SST) application. The requirement for flexible power sharing control, methodology for voltage balance and power sharing control are discussed. Finally, experimental results are presented for the validation.

4.1 Requirement for Flexible Power Sharing Control

The modular SST serves as an interface between MVAC distribution grid and LVDC distribution system. Ensuring voltage balance and power balance across the cells of a modular SST is crucial for any control scheme. Fig. 4.1 shows this modular SST topology in ISOP configuration. Imbalances in power and voltage typically result from mismatches in the



(a) Modular SST converter in ISOP configuration.



(b) Circuit diagram of n^{th} cell.

Figure 4.1: Circuit diagram of modular 1-phase type-D SST topology.

value of cell-to-cell HF-link inductance and transformer turns ratio in the DAB stage. The variation of HF-link inductance values is of greater significance, as it directly impact the power transfer. In contrast, the turns ratio remains a fixed physical designed parameter determined solely by the number of turns [61]. While parametric mismatches also exist in the switching devices and DC-link capacitors, it is the HF-link inductance that primarily influences the power transfer. Unequal distribution of power and voltage result in uneven device stress, irregular heat dissipation and high distortion in current drawn from the grid, which are undesirable. Non-uniform thermal loading may result in accelerated ageing or premature failure of the active devices, compromising the reliability of the system. Therefore, it is necessary to devise the control architecture in such a way that it guarantees equal sharing of power and MVDC bus voltages, even in the presence of parameter mismatches across different SST cells. The proposed control scheme ensures equal power and voltage sharing between cells to mitigate the aforementioned issues. Furthermore, it can also

facilitate controlled unequal power sharing when necessary, in contrast to erstwhile methods. This capability is particularly beneficial during light load or fault conditions, enabling seamless plug-out (phase-shedding) and plug-in (phase-addition) operations. As this control scheme is capable of both equal and controlled unequal power sharing, in this research work it is referred as flexible power sharing control. This flexible power sharing feature can play a pivotal role during contingency situations, such as fault conditions and maintenance of a cell. In such cases, the concerned cell can be quickly deactivated by reducing its power transfer to zero, allowing the remaining cells to operate near their rated power. A comprehensive comparison with previously established strategies is provided next.

4.2 Functional Comparison with Other Reported Schemes

The briefly discussed control schemes in Chapter 1, categorised as strategy A, B and C are compared here and elaborated upon extensively. In [47], an early implementation of strategy A is documented. However, a significant drawback of this approach is its reliance on costly high-bandwidth (HBW) current sensors and ADCs with high sampling rates to measure and sample each HF link inductor currents. The study referenced in [62] uses a three-phase power balance and MVDC balance controller in the CMFEC. However, it does not account for parametric uncertainty in the HF link.

To obviate the necessity for these HBW sensors, a coordinated control strategy is introduced in [48, 49] which falls under strategy B. Nevertheless, the dynamic performance of MVDC links in these methods exhibits sluggishness, with settling times exceeding 50 grid cycles. In [63], a model predictive control method is introduced to attain power balance for ISOP-DAB in a power electronic traction transformer (PETT). However, it pre-assumes the HF-link inductance values and overlooks parametric uncertainties arising from ageing.

An initial work based on strategy C is documented in [64], where a uniform duty cycle is applied to all FECs. The power balance strategy commonly employed for DABs operating

in ISOP mode are documented in [52], [65], [66]. In [53], a dual phase shift (DPS) PWM technique is introduced, presenting a dual control loop for the DAB stage. In [54], a voltage balancing technique is introduced for PETT in traction applications, while [55] proposes a similar technique for smart transformers. These approaches require assigning an identical duty cycle to all FECs in the CMFEC to control the summation of MVDCs and individually regulate MVDC voltages in the DAB stage. However, the effect of load disturbances on the dynamic response of MVDCs remains a concern, given that both MVDCs and LVDC are regulated by the same central control structure.

Across all these approaches categorized under strategy C, the control framework relies on the simplified reduced order model of DAB, omitting the HF-link current (i_{Ls}) as a state variable. Moreover, since all FEC modules in CMFEC are allocated the same modulation duty cycle, this control strategy inherently restricts its utilization of the full degrees of freedom available within the topology. Hence, it lacks the capability to implement flexible power sharing, which is one of its shortcomings. Recent works have focused on enhancing the dynamics of MVDC voltages through the implementation of power-linked model predictive control (PLPC) [67]. However, there is a lack of experimental results demonstrating unequal or zero power sharing. In [68, 69], a predictive control approach for fault-tolerant conditions is introduced, although the transient dynamic performance is not addressed.

Therefore, the aim is to develop a control strategy that facilitates flexible power sharing by directly controlling the fundamental component of HF-link current, without measuring it. A comparison between the proposed control scheme and other approaches, is outlined in Table 4.1. The overall control objectives here are,

1. Achieving unity power factor (UPF) operation on the grid side (MVAC side).

2. Regulating the total summation of MVDC voltages.

3. Balancing individual MVDC voltages.

Table 4.1: Comparison of control schemes for modular SST in ISOP configuration.

Reference	Strategy	Control of i_{Ls} fundamental component	HBW Sensor	Controlled flexible power sharing	Approx. MVDC settling time $*$
[47]	A	Yes	Yes	Both equal unequal and zero $\diamond$	4-5
[62]	A	No	No †	Only equal	12
[70]	A	No	No †	Both equal unequal and zero $\diamond$	NA
[48, 49]	B	No	No	Only equal	> 50
[64]	C	No	No †	Only equal	NA
[53]	C	No	No	Only equal	25 §
[54]	C	No	No	Only equal	28
[55]	C	No	No †	Only equal	3
[56]	C	No	No	Only equal	12 §
[63]	MPC	No	No †	Only equal	NA
[67]	PLPC	No	No	Only equal	3
[68]	PLPC	No	No	Both equal unequal and zero $\diamond$	NA
Proposed	A	Yes	No	Both equal unequal and zero $\diamond$	3-4

$\diamond$ Zero power sharing = Phase-shedding/plug-out operation. $*$ In grid cycles (For sudden load variation)
§ For power reversal. † Equal/Known inductance in DAB HF-Link, NA - Not available.

4. Maintaining power balance by ensuring equal throughput power delivery across all cells, regardless of parametric variation in L_s, in normal situation.

5. Achieving flexible power sharing during contingency situations.

6. Regulating the output voltage (v_o).

In the subsequent sections of this chapter, the proposed control of modular SST and its working is discussed.

4.3 Voltage Balance Control

The objective of MVDC voltage balancing is accomplished in the CMFEC control stage in the proposed strategy. In Chapter 2, the dynamic equations for the CMFEC stage are derived and shown in (2.4), (2.5) and (2.6). Applying KVL, the summation of pole voltages (v_{pT}) and pole voltage of k^{th} FEC (v_{pk}) can be derived as,

$$v_{pT} = \sum_{k=1}^{n} v_{pk} = v_g - j\omega L_g i_g, \tag{4.1}$$

$$v_{pk} = (d_{dk} + jd_{qk})v_{dck}. \tag{4.2}$$

Substituting (4.2) into (4.1) and rearranging the real and imaginary terms, (4.3) can be derived.

$$\sum_{k=1}^{n} d_{dk} v_{dck} = v_g. \tag{4.3a}$$

$$\sum_{k=1}^{n} d_{qk} v_{dck} = -\omega L_g i_g. \tag{4.3b}$$

The active power transfer in a k^{th} FEC and the k^{th} DAB can be represented as,

$$P_{feck} = i_{gd} v_{dck} = i_g d_{dk} v_{dck}, \tag{4.4}$$

$$p_{dabk} = \frac{N_{tk} v_o v_{dck}}{2 f_s} \frac{1}{L_{sk}} d_{\varphi k}(1 - d_{\varphi k}). \tag{4.5}$$

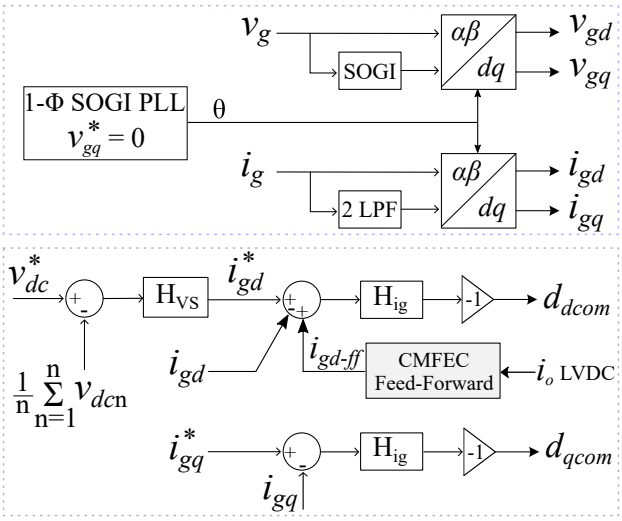
Under the assumption of a lossless system, the active power transfer in the k^{th} FEC and k^{th} DAB remains identical since they are both connected in series. Due to the series connection of the cascaded multilevel rectifier, the current flowing through each FEC is also same (i_g). From (4.4), it can be inferred that equalization of the term, $d_{dk} v_{dck}$, signifies equal power sharing among the FEC modules of CMFEC. Consequently, this also denotes power

balance within SST cells, as each FEC output is linked to the corresponding DAB input in series. Similarly, the terms N_{tn}, v_o, f_s are same for all DABs. Equating (4.4) to (4.5) the relationship between FEC control input and DAB control input is established as,

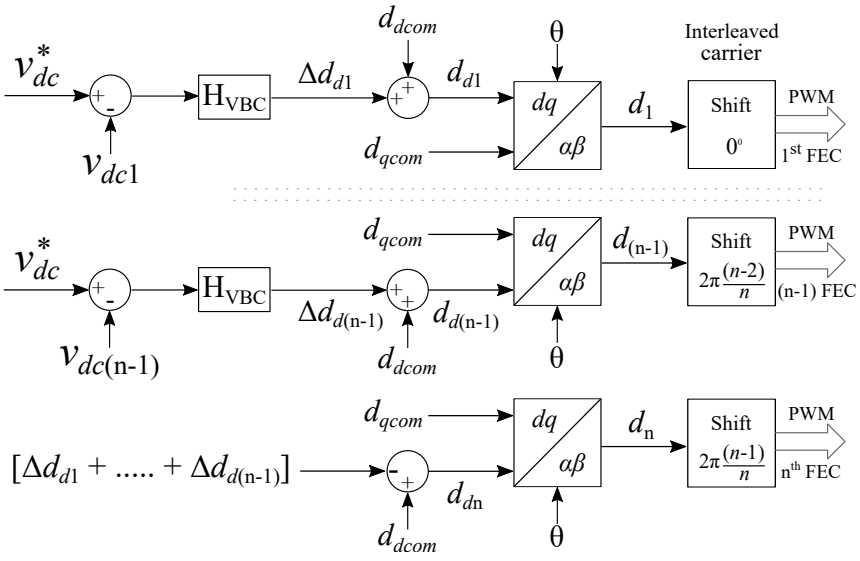
$$d_{dk} \propto \frac{1}{L_{sk}} d_{\varphi k}(1 - d_{\varphi k}). \tag{4.6}$$

This equation clearly suggests that any parametric uncertainty in the DAB stage, due to unequal values of L_{sk}, can be compensated by the control input $d_{\varphi k}$. Hence, in the power balance state, d_{dk} remains constant for all FECs.

As previously mentioned, the term $d_{dk}v_{dck}$ is proportional to the power flow through an FEC. To satisfy the requirement of voltage balance, all MVDC voltages should be equal. On the other hand, if unequal power distribution among the FECs is desired by keeping the voltage balance intact, the control signal which needs to be modified is d_{dk}. This key control variable makes both equal and unequal power sharing, i.e, flexible power sharing possible. This is fundamental idea behind this work. The voltage balance controller should generate compensated d_{dk} for each FEC so that the MVDC voltages remain equal even in the presence of power imbalances. For instance, during equal power sharing, the controllers produce equal d_{dk} values for all FECs. During controlled unequal power sharing, the controller adjusts d_{dk} based on power distribution. In scenarios like plug-out/phase-shedding operation of k^{th} cell, the controller generates $d_{dk} = 0$, while modifying $d_{d1}, d_{d2}, ...d_{d(k-1)}$ by a factor of $k/(k-1)$. The overall control scheme for CMFEC stage is shown in Fig. 4.2. To meet the grid side objective, traditional 1-phase vector control scheme based on the dq-model is employed. At the start, v_g is oriented along the d-axis by ensuring $v_{gq} = 0$, by using a phase-locked loop (PLL) based on SOGI. Consequently, the d-axis and q-axis components becomes associated with active and reactive power respectively. For UPF operation, the reference for the reactive component of grid current ($i^*_{gq} = 0$) is set to zero. The outer voltage loop keeps the sum of MVDC voltages ($\sum v_{dcn}$) constant by directly control-



(a) Vector control and common duty generation.



(b) CMFEC stage voltage balance control.

Figure 4.2: Control scheme for the CMFEC stage.

ling its average value. Meanwhile, the inner current loop produces the active (d_{dcom}) and reactive (d_{qcom}) components of the common duty ratio (d_{com}). Subsequently to meet the objective of equal MVDC voltage sharing, this common active component is summed with the output of the dedicated voltage balance controller (H_{VBC}) for each cell. This combination generates the adjusted duty ratio unique to each cell, as described in [47]. For the n^{th} FEC, this component is denoted as (d_{dn}). Since d_{dcom} is common for all FECs, the

only component capable of inducing inequality in d_{dn} is Δd_{dk}. As previously mentioned, the output of H_{VBC} controller, Δd_{dk}, serves as the crucial control parameter that enables flexible power sharing by directly controlling the individual MVDC voltages.

4.3.1 Proposed Feed-forward Compensator for CMFEC

In the event of sudden load fluctuations at the LVDC side, the MVDC voltages are directly affected, consequently impacting both grid-side and load-side operations. Therefore, to enhance the disturbance rejection capability of the entire control system, a feed-forward compensation method is introduced. A feed-forward term is formulated to establish a connection between the DAB load-side current (i_o) and the CMFEC grid-side current (i_{gd}) in the following manner. Equation (4.3) is reproduced here,

$$v_g = \sum_{k=1}^{n} d_{dk} v_{dck} = d_{d1} v_{dc1} + d_{d2} v_{dc2} + ... + d_{dn} v_{dcn}. \tag{4.7}$$

Substituting the respective $d_{dk} = d_{dcom} + \Delta d_{dk}$ for each FEC in the CMFEC, (4.7) can be rearranged and expressed as,

$$[(v_{dc1} + v_{dc2} + ... + v_{dcn}) d_{dcom}] + [v_{dc1} \Delta d_{d1} + v_{dc2} \Delta d_{d2} + ... + v_{dcn} \Delta d_{dn}] = v_g. \tag{4.8}$$

In the above equation, both v_g and d_{dcom} are common and identical for all FECs. Once the MVDC voltage balance is attained, it results in $v_{dc1} = v_{dc2} = \ldots = v_{dcn} = v_{dc,avg}$. Substituting this in (4.8), it can be rewritten as,

$$[n v_{dc,avg} d_{dcom}] + [v_{dc,avg} (\Delta d_{d1} + \Delta d_{d2} + ... + \Delta d_{dn})] = v_g. \tag{4.9}$$

The only term subject to perturbation or variation in the given equation is Δd_{dk} based on power distribution among the FECs. Segregating and arranging the large signal terms

and perturbed terms of equation (4.9) leads to,

$$nv_{dc,avg}d_{dcom} = v_g, \quad \text{and} \quad v_{dc,avg}(\Delta d_{d1} + \Delta d_{d2} + ... + \Delta d_{dn}) = 0. \tag{4.10}$$

Equation (4.10) can be further simplified to arrive at,

$$d_{dcom} = \frac{1}{n}\Big[\sum_{k=1}^{n} d_{dk}\Big] = \frac{v_g}{nv_{dc,avg}}, \quad \text{and} \quad \sum_{k=1}^{n} \Delta d_{dk} = 0. \tag{4.11}$$

Neglecting the losses and the switching frequency components, a relation between i_{gd} and i_o is derived as,

$$i_{dcn} = d_{dn}i_{gd} = i_{1n} = i_{2n}/N_{tn} = i_o/(nN_{tn}), \tag{4.12}$$

$$i_{gd} = i_o/(nN_{tn}d_{dcom}), \tag{4.13}$$

where, i_{dcn}, i_{1n} and i_{2n} represent the FEC DC-link output current, DAB DC-link input current and DAB DC-link output current in the n^{th} cell, respectively. Substituting d_{dn} with d_{dcom} accounts for the average impact across all cells and simplifies hardware realization. Therefore, the relationship outlined in (4.13) is utilized to derive the feed-forward term. To establish the dynamic relationship between i_{gd} and i_o, (4.13) is linearized by introducing a small perturbation, resulting in,

$$\tilde{i}_{gd} = \frac{1}{nN_{tn}D_{dcom}}\tilde{i}_o - \frac{I_o}{nN_{tn}{D_{dcom}}^2}\tilde{d}_{dcom}. \tag{4.14}$$

In this equation, the first term connects the perturbation in i_o with the perturbation in i_{gd}. This represents the feed-forward term (i_{gd-ff}), which can be expressed as follows,

$$\tilde{i}_{gd-ff} = \tilde{i}_o/(nN_{tn}D_{dcom}). \tag{4.15}$$

D_{dcom} represents the nominal value of the common active component of the CMFEC duty

ratio at full load. The nominal value of D_{dcom} can be obtained as,

$$D_{dcom} = V_{gd}/(nN_{tn}V_o). \tag{4.16}$$

The subsequent section addresses power balance control in the modular DAB stage.

4.4 Sensorless Power Balance Control

As noted earlier, the parameter which is primarily responsible for unequal power distribution among the SST cells is the mismatch in the values of HF-link inductance (L_s) from one cell to another. This is clearly evident from the DAB power equation presented in (4.5). The control objectives are achieved in this proposed current sensorless scheme by utilizing the estimated value of the fundamental component of the HF-link inductor current (i_{Ls}). Before proceeding, it is necessary to estimate L_{sn} in each cell, a topic to be discussed in the subsequent subsection. Here, the power balance strategy is introduced under the assumption that L_{sn} has been estimated with satisfactory accuracy.

This study introduces a power balance strategy based on the estimation of HF-link current fundamental component, facilitated by online parameter identification and its updation. State observers are designed to estimate the DAB current fundamental envelopes, enabling control actions to achieve power balance. The small-signal model of the n^{th} DAB cell is formulated using GA modeling, as shown in (4.17), with state variables including $\langle v_o \rangle_0$, $\langle i_{Lsn} \rangle_1^R$ and $\langle i_{Lsn} \rangle_1^I$ [71].

The dominant component of the Fourier series of i_{Ls} is its fundamental frequency term. Therefore, controlling its active power component in each DAB results in power balance across the SST cells. This analysis applies fundamental harmonic approximation. The expression for the fundamental component of active power (p_{fund_n}) in the n^{th} DAB is

$$\underbrace{\begin{bmatrix} \langle \dot{\tilde{v}}_o \rangle_0 \\ \langle \dot{\tilde{i}}_{Lsn} \rangle_1^R \\ \langle \dot{\tilde{i}}_{Lsn} \rangle_1^I \end{bmatrix}}_{\dot{\tilde{\mathbf{x}}}_n} = \underbrace{\begin{bmatrix} \frac{-1/n}{R_o C_o} & -\frac{4N_{sin}}{\pi C_o} & -\frac{4N_{cos}}{\pi C_o} \\ \frac{2N_{sin}}{\pi L_{sn}} & -\frac{R_{sn}}{L_{sn}} & \omega \\ \frac{2N_{cos}}{\pi L_{sn}} & -\omega & -\frac{R_{sn}}{L_{sn}} \end{bmatrix}}_{\mathbf{A}_n} \underbrace{\begin{bmatrix} \langle \tilde{v}_o \rangle_0 \\ \langle \tilde{i}_{Lsn} \rangle_1^R \\ \langle \tilde{i}_{Lsn} \rangle_1^I \end{bmatrix}}_{\tilde{\mathbf{x}}_n} + \underbrace{\begin{bmatrix} \frac{4}{C_o}\big[N_{sin} I_{Ls1In} - \\ N_{cos} I_{Ls1Rn}\big] \\ \frac{2N_{cos}}{L_{sn}} V_o \\ -\frac{2N_{sin}}{L_{sn}} V_o \end{bmatrix}}_{\mathbf{B_{1n}}} \underbrace{\tilde{d}_{\varphi n}}_{u_{1n}} - \underbrace{\begin{bmatrix} 0 \\ 0 \\ \frac{2}{\pi L_{sn}} \end{bmatrix}}_{\mathbf{B_{2n}}} \underbrace{\tilde{v}_{dcn}}_{u_{2n}} - \underbrace{\begin{bmatrix} \frac{1}{nC_o} \\ 0 \\ 0 \end{bmatrix}}_{\mathbf{B_{3n}}} \underbrace{\tilde{i}_N}_{u_{3n}} \tag{4.17}$$

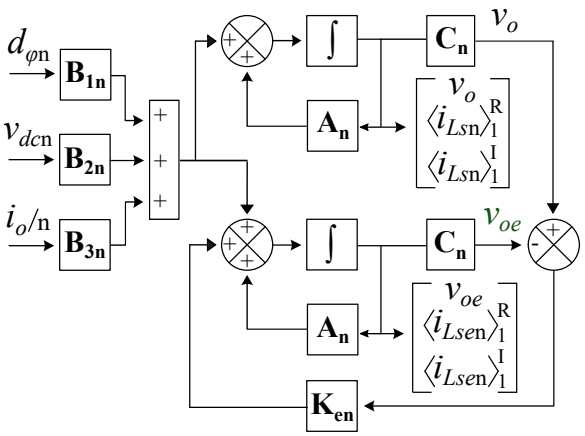
previously derived in Chapter 3 and reproduced here as,

$$p_{fund\_n} = 2\big[\langle v_{prin} \rangle_1^R \langle i_{Lsn} \rangle_1^R + \langle v_{prin} \rangle_1^I \langle i_{Lsn} \rangle_1^I\big] = -\frac{4}{\pi} \langle v_{dcn} \rangle_0 \langle i_{Lsn} \rangle_1^I. \tag{4.18}$$

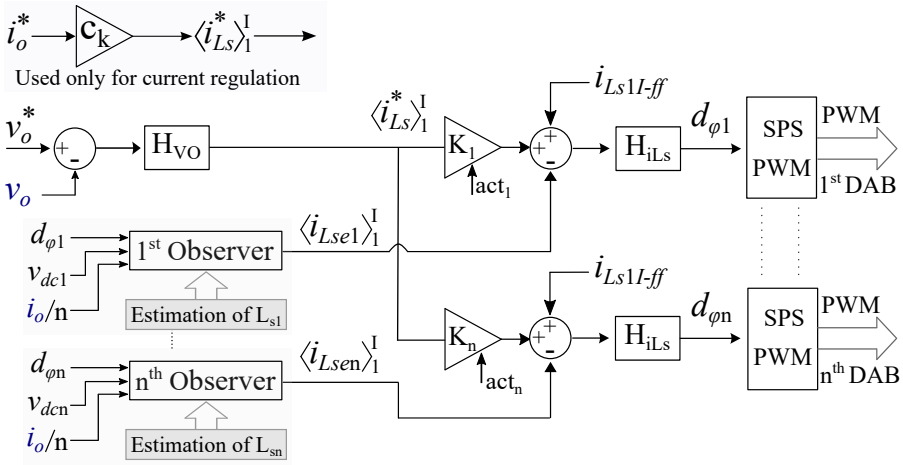
As apparent from (B.7), $\langle i_{Lsn} \rangle_1^I$ represents the active power component of the inductor current, making it a chosen control variable alongside v_o.

The block diagram of the proposed estimation-based control scheme is depicted in Fig. 4.3. It comprises a dual-loop control system consisting of an outer voltage and an inner current loop. The outer loop is responsible for regulating v_o. The H_{VO} controller generates the current reference for all DABs. Following this, the inner loop comparator compares the $\langle i_{Ls}^* \rangle_1^I$ reference with the estimated $\langle i_{Lsen} \rangle_1^I$ obtained from the state observer block of n^{th} DAB. Subsequently, the current controller (H_{iLs}) generates the phase shift duty ratio $d_{\varphi n}$ for the n^{th} DAB module. A feed-forward compensation term is introduced into each inner current loop of the modular DAB to improve its dynamic response. The feed-forward term ($i_{Ls1I-ff}$) is derived as,

$$i_{Ls1I-ff} = \Big[\Big\{\frac{1}{n}\sum_{k=1}^{n} \langle i_{Lsen} \rangle_1^I\Big\} - I_{Ls1I\_nom}\Big], \tag{4.19}$$



(a) n^{th} DAB state observer block.



(b) Daul loop control with HF-link inductance estimation.

Figure 4.3: Observer based power balance control in modular DAB stage.

where, I_{Ls1I_nom} can be obtained as,

$$I_{Ls1I\_nom} \approx \frac{\pi}{2\cos\Phi_{nom}} \times \frac{I_o}{n}. \tag{4.20}$$

Here, Φ_{nom} represents the nominal phase shift angle between the two H-bridges of DAB.

The observer block is depicted in Fig. 4.3a. In the ISOP configuration, all DAB modules share the same output voltage v_o as they are connected in parallel. However, due to cell-to-cell parametric variation, the discrepancy between measured v_o and estimated v_{oen} in the state observer of n^{th} DAB varies among cells. Consequently, the observer gain ma-

trix for each DAB differs, depending on the magnitude of estimation error. The observer gain matrix for n^{th} DAB is denoted by $\mathbf{K_{en}}$. Mathematical model of n^{th} DAB module full order state observer is given in (4.21), where $\mathbf{x}_{en} = \begin{bmatrix} \langle v_{oen} \rangle_0 & \langle i_{Lsen} \rangle_1^R & \langle i_{Lsen} \rangle_1^I \end{bmatrix}^T$, are the estimated state variables corresponding to n^{th} DAB.

$$\dot{\mathbf{x}}_{en} = (\mathbf{A}_n - \mathbf{K_{en}}\mathbf{C}_n)\mathbf{x}_{en} + \mathbf{B_{1n}}d_{\varphi n} + \mathbf{B_{2n}}v_{dcn} + \mathbf{B_{3n}}i_N + \mathbf{K_{en}}v_o. \tag{4.21}$$

The estimated state $\langle i_{Lsen} \rangle_1^I$ varies across different DAB modules depending on their respective $d_{\varphi n}$ and L_{sn} values. This estimated state serves as the feedback input to the inner current control loop of the n^{th} DAB. The inner current controller H_{iLs} generates distinct $d_{\varphi n}$ for each DAB cell based on the disparity in the feedback of $\langle i_{Lsen} \rangle_1^I$, aiming to achieve power balance in the modular SST.

This control scheme also allows current mode control for the regulation of output current (i_o). In the course of current regulation, the outer voltage loop can be disabled, and the LVDC side load current reference (i_o^*) can be directly provided with a multiplication factor C_k as illustrated in Fig. 4.3.

$$C_k = \pi/(2n \cos \Phi_{nom}). \tag{4.22}$$

Additionally, deactivating a specific cell is facilitated by setting the corresponding gain k_n (shown in Fig. 4.3) to zero using the act_n input. This functionality allows for the phase-shedding operation of that cell. It makes flexible power sharing possible during fault condition or low load periods.

4.4.1 HF-Link Inductance estimation

Various schemes for identifying the HF-link inductance value of a single-cell DAB are discussed [61, 71, 72]. This study presents an inductance estimation scheme for output parallel-connected DABs in modular ISOP SST. The basis of the inductance estimation

scheme lies in equating the active component of the input current of the n^{th} DAB, with the active component of the output current of its series-connected n^{th} FEC. This forms the foundation of the modular SST inductance estimation approach. The derivation of HF-link inductance value is provided subsequently.

The output current (i_{dcn}) of the n^{th} FEC cell can be expressed as,

$$\begin{aligned} i_{dcn} = i_g d_n = (i_{gd} + j i_{gq})(d_{dn} + j d_{qn}) = \\ (i_{gd} d_{dn} - i_{gq}.d_{qn}) + j(i_{gd} d_{qn} + i_{gq} d_{dn}). \end{aligned} \tag{4.23}$$

Considering the UPF operation at the grid side, the reactive component of the current, i_{gq}, equals to 0. Substituting this into (4.23), active component of i_{dcn} can be derived as,

$$i_{dcn\_active} = i_{gd} d_{dn}. \tag{4.24}$$

Using the throughput power expression of a DAB converter with SPS PWM technique, the active current input of the DAB module in the nth cell can be found as,

$$i_{1n} = \frac{N_t v_o}{2 f_s L_{sn}} d_{\varphi n}(1 - d_{\varphi n}), \tag{4.25}$$

By equating (4.24) with (4.25), the inductance value in the n^{th} DAB module can be determined as,

$$L_{sn} = \frac{N_t v_o}{2 f_s d_{dn} i_{gdn}} d_{\varphi n}(1 - d_{\varphi n}). \tag{4.26}$$

In the implementation of the control scheme, the inductance estimation loop is integrated to the control architecture as illustrated in Fig. 4.3. Detailed step-by-step working of the control scheme is elucidated in the subsequent subsection.

4.4.2 Step-by-step Working of the Control Scheme

In this section, the operational workflow of the proposed control scheme is presented sequentially to aid in comprehending the entire process. This is represented in a flowchart, as depicted in Fig. 5.7. In terms of the sequence of successive events, the operation can be categorized into three distinct steps.

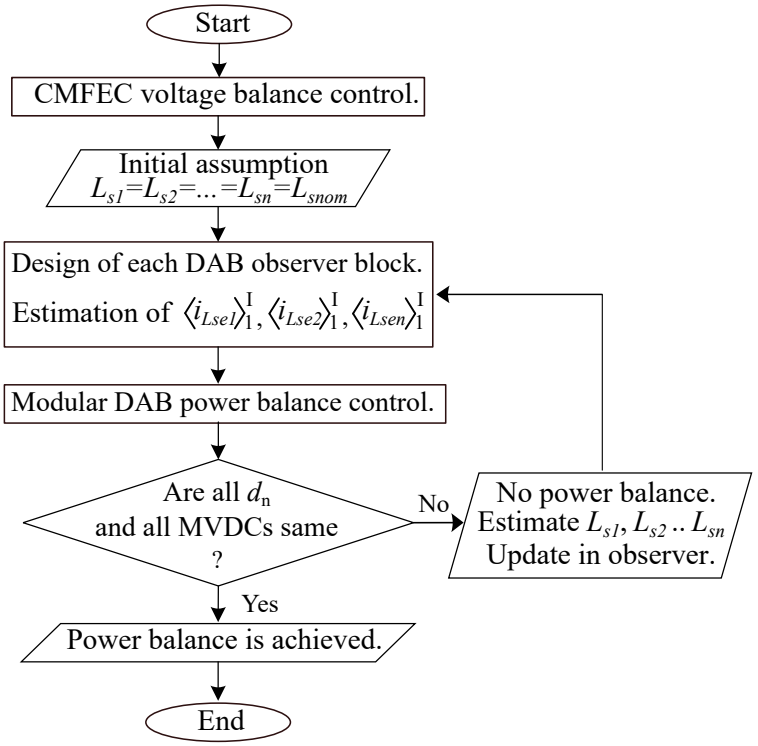


Figure 4.4: Control scheme flowchart showing step by step working.

The first step of this proposed control strategy commences by powering up the system with CMFEC-based voltage balance control. This guarantees MVDC voltage balance by equalizing $v_{dc1} = v_{dc2} = .. = v_{dcn}$. In the DAB stage, various cells might possess distinct HF-link inductance values owing to plant uncertainty, which remain undisclosed at this juncture. However state observer block of each DAB operates under the assumption that L_s for every cell is equal to the nominal/nameplate rating (L_{snom}), implying $L_{s1} = L_{s2} = .. = L_{sn} = L_{snom}$. Thus, the same nominal control inputs are initially applied to all

observer blocks, which is $d_{\varphi 1} = d_{\varphi 2} = .. = d_{\varphi n} = d_{\varphi nom}$. Consequently, the output of every observer block is identical, resulting in $\langle i_{Lse1} \rangle_1^I = \langle i_{Lse2} \rangle_1^I = .. = \langle i_{Lsen} \rangle_1^I$. Given that identical estimated values are provided as feedback to each respective inner current loop, the H_{iLs} current controllers in each inner loop generate identical phase shift duty ratios, that is $d_{\varphi 1} = d_{\varphi 2} = .. = d_{\varphi n}$. As a result, due to the variation in L_s from cell-to-cell, power balance cannot be attained at this point. This power imbalance directly influences the unequal modulation duty ratio of each FEC stage, indicated by $d_1 \neq d_2 \neq .. \neq d_n$. This outcome is inevitable since MVDC voltage balance is achieved, yet the active component of the current varies from cell-to-cell. Considering that all FEC cells share the same grid current i_g, this is the only conceivable result at this stage unless all L_s values are equal.

During step 2, the inductance values in each DAB are estimated using (4.26). Subsequently, these values are updated in the respective state observer blocks to estimate $\langle i_{Lse} \rangle_1^I$ of each DAB.

In step 3, if there are discrepancies in the values of L_s across cells, the estimated state $\langle i_{Lse} \rangle_1^I$ differs for each observer block. These estimated values are then provided as feedback to their respective inner current control loop. Accurate estimation of inductances inherently results in precise estimation of $\langle i_{Lse} \rangle_1^I$. Consequently, this minimizes the current error in each loop, thereby facilitating the achievement of power balance across cells. If L_s are different across cells, it inevitably leads to $d_{\varphi 1} \neq d_{\varphi 2} \neq .. \neq d_{\varphi n}$. Moreover, upon achieving both voltage balance and power balance, the duty ratio of all FECs, which initially differed at the outset of step 1, now becomes equal. Consequently, by the conclusion of step 3, $d_1 = d_2 = .. = d_n$. Once power balance is attained, the inductance estimation block can be deactivated and reactivated as needed when the duty cycle in the FEC stage becomes unequal. This implementation approach effectively mitigates the effects of parametric uncertainty arising from ageing.

4.5 Results and Discussion

Experimental validation was conducted using a low power hardware prototype of a 1.6 kW modular SST with two number of cells, as depicted in Figure 4.5. The experimental system parameters are detailed in Table 4.2. Discrete IGBT devices (IKQ50N120CT2) are used in the power stage of the SST, whereas ISO5852S isolated gate driver ICs were selected for driving the IGBTs. Two current sensors were employed during experiment to measure the DC output current (i_o) and AC grid current (i_g), with their respective bandwidths provided in Table 4.3. The digital control platform utilized for the experiment comprised DSP microcontroller TMS320F28377S and SPARTAN-6 FPGA.

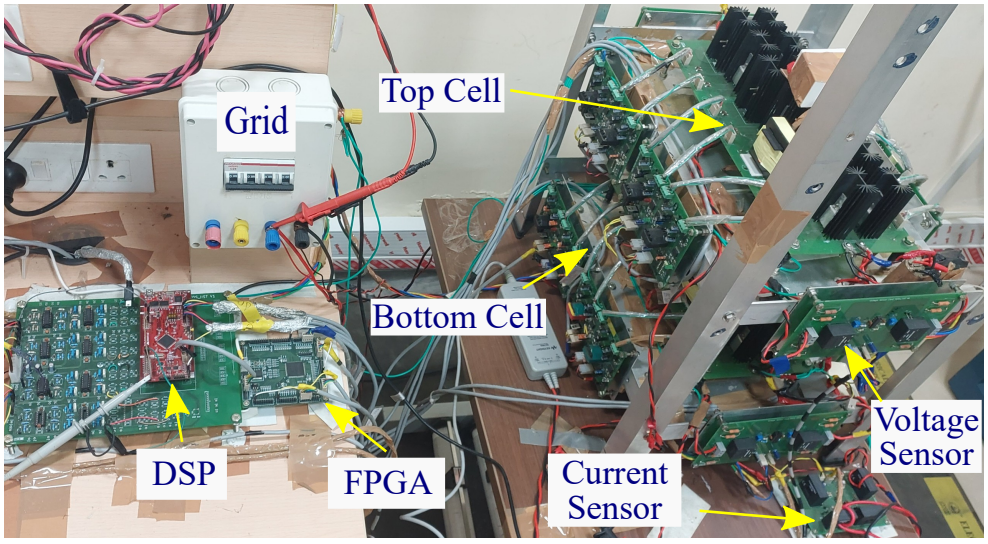


Figure 4.5: Hardware Prototype of 2 cell type-D SST.

The nominal rating for the DAB cell inductances is $150\mu H$ as per the nameplate. However, to account for parametric uncertainty, two inductors with values of $130\mu H$ and $177\mu H$ were specifically chosen as L_{s1} and L_{s2} respectively. Thus, the inductance values for the experiment were deliberately selected with a $\pm 15\%$ variation from the nominal value. The high frequency link transformers were designed with a turns ratio of 0.8 for both cells. Initially, the goal was to confirm the effectiveness of the voltage balance control in

Table 4.2: Experiment Parameters

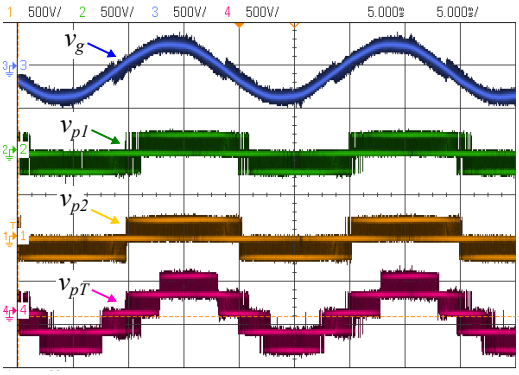
Parameter	Symbol	Value
DAB 1, 2 inductance	L_{s1}, L_{s2}	130, 177 μH
LVDC Capacitance	C_o	470 μF
MVDC 1, 2 Capacitance	C_1, C_2	2.2 $\pm$10% mF
DAB Switching frequency	f_{DAB}	20 kHz
FEC Switching frequency	f_{FEC}	4 kHz
HF link turns ratio	N_{tn}	4:5
Rated MVDC voltage	V_{dcn}	205 V
Rated LVDC voltage	V_o	255 V
Grid input voltage (RMS)	v_g	220 V, 50 Hz
Grid interfacing inductance	L_g	6 mH
Load Resistance	R_o	40 Ω
Total power	P_t	1.6 kW

Table 4.3: Bandwidth of sensors used in this work.

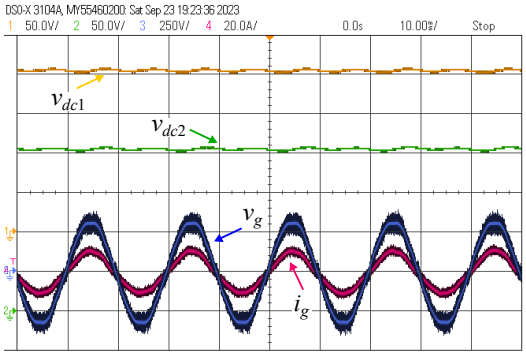
Measured Parameter	Sensor*	Bandwidth
v_g, v_o, v_{dc1}, v_{dc2}	HA025T01	Low – 200 kHz
i_g, i_o	VH1K0T01	Low – 200 kHz

$*$ Make - Electrohms Private Limited

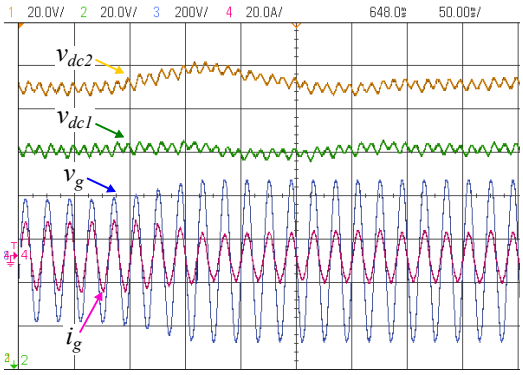
the CMFEC stage without activating the L_s estimation blocks. The experimental findings are depicted in Figure 4.6. To achieve carrier-based interleaving PWM, the carrier signals of FEC1 and FEC2 were phase-shifted by 90°. This enables multilevel operation, with v_{p1} and v_{p2} representing the switched pole voltages of FEC1 and FEC2 at 2 levels, while the total pole voltage v_{pT} consists of 5 levels. The corresponding outcomes are depicted in Figure 4.6a. Additionally, the experimental result demonstrating UPF operation, where v_g and i_g are in phase, is shown in Figure 4.6b. The two MVDC voltages v_{dc1} and v_{dc2} are displayed, with peak-to-peak voltage ripple approximately 3.5%. Both MVDC voltages,



(a) Multilevel operation of CMFEC.



(b) UPF Operation of CMFEC.



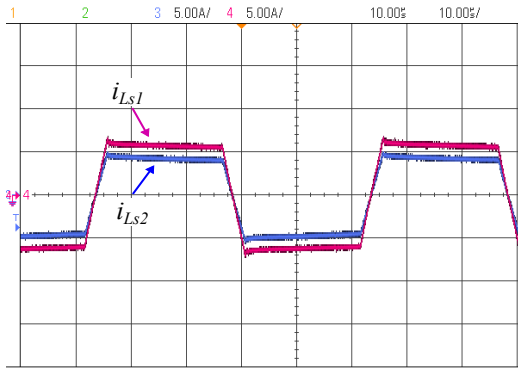
(c) Grid line voltage disturbance rejection.

Figure 4.6: Experimental results showing voltage balance control of CMFEC. (a) Top trace: v_g (500 V/div), 2nd trace: v_{p1} (500 V/div), 3rd trace: v_{p2} (500 V/div), Bottom trace: v_{pT} (500 V/div). (b) Top trace: v_{dc1} (20 V/div), 2nd trace: v_{dc2} (20 V/div), Bottom trace: v_g (200 V/div) and i_g (20 A/div). (c) Top trace: v_{dc2} (20 V/div), 2nd trace: v_{dc1} (20 V/div), Bottom trace: v_g (200 V/div) and i_g (20 A/div). Time:- (a) 5 ms/div, (b) 4 ms/div, (c) 50 ms/div.

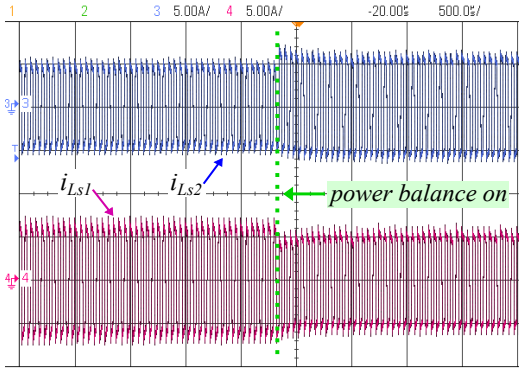
are confirmed to be equals to 205 volts. This confirms the effectiveness of voltage balance control, even in the presence of $\pm 15\%$ variation in HF-link inductances in the DAB stage. The dynamic performance of the voltage balance control was evaluated by subjecting v_g to voltage variation in a ramp manner, transitioning from 200 V to 265 V, as depicted in Figure 4.6c. Both MVDC voltages effectively reject the disturbance, maintaining variation within $\pm 5\%$ during the transient. As v_g increases, i_g decreases accordingly, all while UPF operation remains intact throughout this transient period, as illustrated in Figure 4.6c.

To assess the effectiveness of the proposed power balance scheme, the HF-link induc-

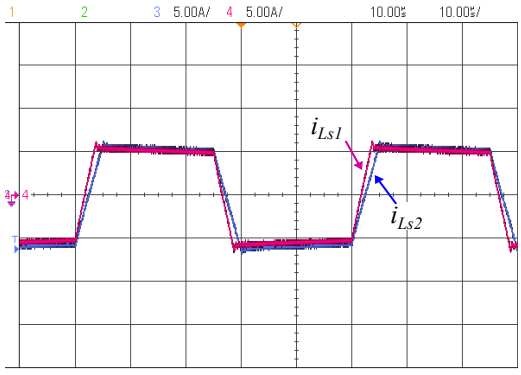
tance and fundamental current estimation blocks were activated separately. The experimental findings are illustrated in Figure 4.7. Figure 4.7a demonstrates that, the two DAB inductor currents i_{Ls1} and i_{Ls2} exhibit inequality in the absence of power balance control. As anticipated, i_{Ls2} is lesser than i_{Ls1} due to the higher actual inductance value of L_{s2} compared to L_{s1}. It was noted that $i_{Ls1,rms}$ and $i_{Ls2,rms}$ deviated to approximately 113.5% and 86.5% respectively from the expected values under power balance. The fundamental harmonic active components, $\langle i_{Lse1} \rangle_1^I$ and $\langle i_{Lse2} \rangle_1^I$, for both DAB cells were estimated to be identical. This was because the state observers for both DAB cells were designed with the same nominal inductance value. Consequently, the corresponding phase shift duty ratio



(a) i_{Lsn} before power balance.



(b) i_{Lsn} transition when power balance is on.



(c) i_{Lsn} after power balance.

Figure 4.7: Experimental results showing DAB inductor currents during power balance. (a) i_{Ls1} (5 A/div), i_{Ls2} (5 A/div). (b) Top trace: i_{Ls2} (5 A/div), i_{Ls1} (5 A/div). (c) i_{Ls1} (5 A/div), i_{Ls2} (5 A/div). Time:- (a) and (c): 10 μs/div, (b) 500 μs/div.

generated by the inner H_{iLs} current controller was equal for both DAB cells, $(d_{\varphi 1} = d_{\varphi 2})$, resulting in no power balance. The values of L_{s1} and L_{s2} were estimated after activating the proposed online inductance estimation scheme, using the equation (4.26). The inductance values were estimated to be $L_{s1e} = 135\mu H$ and $L_{s2e} = 184\mu H$. The percentage error in the estimation of inductance values was within the range of $\pm 5\%$. After the estimation process, these estimated inductance values were incorporated into their respective state observer blocks. As a result, the observer blocks calculated $\langle i_{Lse1} \rangle_1^I$ and $\langle i_{Lse2} \rangle_1^I$, which were now distinct, and they are fed back to the inner current control loop. The outer voltage controller H_{VO} produced identical reference i^*_{Ls1I} for all the inner current loops. The inner controller H_{iLs} produced distinct $d_{\varphi 1}$ and $d_{\varphi 2}$ values for the two DAB cells in order to minimize the error between $\langle i_{Lse1} \rangle_1^I$, $\langle i_{Lse2} \rangle_1^I$ and the reference i^*_{Ls1I}. Equalising the fundamental active components $\langle i_{Lse1} \rangle_1^I$ and $\langle i_{Lse2} \rangle_1^I$ ensures that i_{Ls1} and i_{Ls2} become nearly equal, given the dominance of the fundamental component in the HF-link current. Eventually, power balance was attained, as confirmed by the experimental results depicted in Figure 4.7c. The waveforms of i_{Ls1} and i_{Ls2} from the pre-power balance to the post-power balance stage is given in Figure 4.7b.

It is evident that upon activation of the power balance scheme, i_{Ls1} reduces while i_{Ls2} increases to quickly approach equality within a few switching intervals. At this point, it was

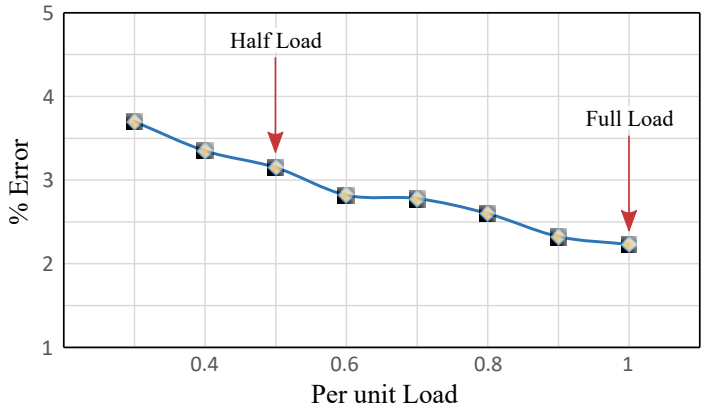
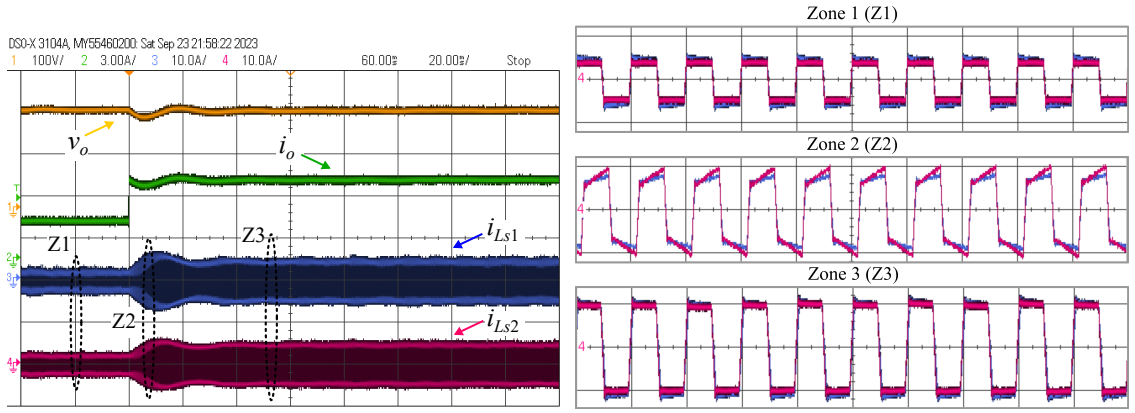


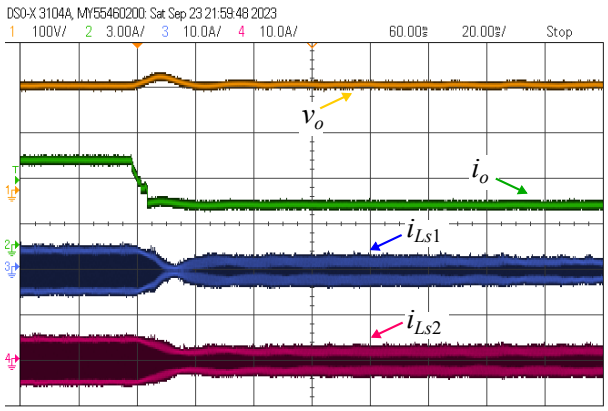
Figure 4.8: Current sharing error with change in load power.

noted that $i_{Ls1,rms}$ and $i_{Ls2,rms}$ were approximately 102.23% and 97.77% respectively of the anticipated values under power balance, resulting in a current sharing error of within 2.23%. Additionally, on the digital control platform, it was observed that upon achieving power balance, the duty cycle of the FEC stage for both cells nearly became equal. Experimental data was gathered and presented in Figure 4.8 to depict the percentage current sharing error relative to variations in load power. The current sharing error remains below 4% across load power variations ranging from full load down to 30% of the full load.



(a) Step increase in load current.

(b) Zoomed view.

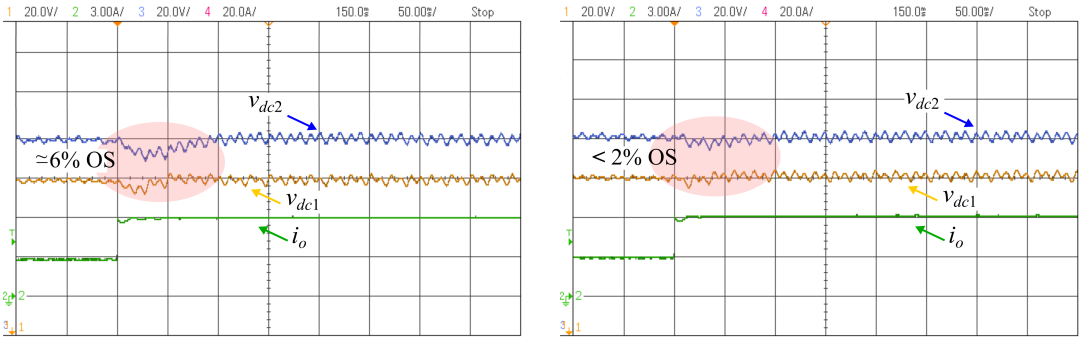


(c) Step decrease in load current.

Figure 4.9: Experimental results during load disturbance. (a) & (c) Top trace: v_o (100 V/div), 2nd trace: i_o (3 A/div), 3rd trace: i_{Ls1} (10 A/div), Bottom trace: i_{Ls2} (10 A/div). (b) Zoomed view of i_{Ls1} and i_{Ls2} shown in (a) with their oscilloscope references superimposed. Upper trace: Zone Z1 of (a), Middle trace: Zone Z2 of (a), Bottom trace: Zone Z3 of (a). Time:- (a) & (c) 20 ms/div, (b) 50 μs/div.

Subsequent experiments were conducted to examine the dynamic behaviour of the proposed control scheme during load transients. The outcomes are presented in Figure 4.9. A load disturbance was introduced by increasing the output load current i_o by 50% from half load to full load (3.1 A $\rightarrow$ 6.2 A). The results shown in Figure 4.9a illustrate that as power balance control is attained, the output current is evenly distributed between L_{s1} and L_{s2}. The time taken for the output voltage v_o to settle is approximately 15 milliseconds with an undershoot of nearly $\pm 5\%$. Following this, a step reduction in the load current i_o was applied as a load disturbance, transitioning from 6.2 A to 3.1 A, and the associated results are depicted in Figure 4.9c. The settling time of v_o is less than 15 ms, with an overshoot within $\pm 5\%$. For enhanced clarity during these transients, enlarged views of the designated zones labeled as Zone1 (Z1), Zone2 (Z2), and Zone3 (Z3) are presented in Figure 4.9b. The experimental results are shown by overlaying the oscilloscope ground reference for i_{Ls1} and i_{Ls2}. A slight variation is noticeable during Z2, corresponding to the transient phase, while both current waveforms are nearly identical before and after this transient.

Subsequently, the experimental results of the step load transients on MVDC voltages are shown. To evaluate the effectiveness of the disturbance rejection, the results are initially presented without the CMFEC stage feed-forward compensation, followed by the



(a) Without feedforward (Zoomed view). **(b)** With feedforward (Zoomed view).

Figure 4.10: Effect of Feed-forward on MVDC voltages. Top Trace: v_{dc2} (20 V/div), middle Trace: v_{dc1} (20 V/div), Bottom Trace: i_o (3 A/div). Time:- 50 ms/div.

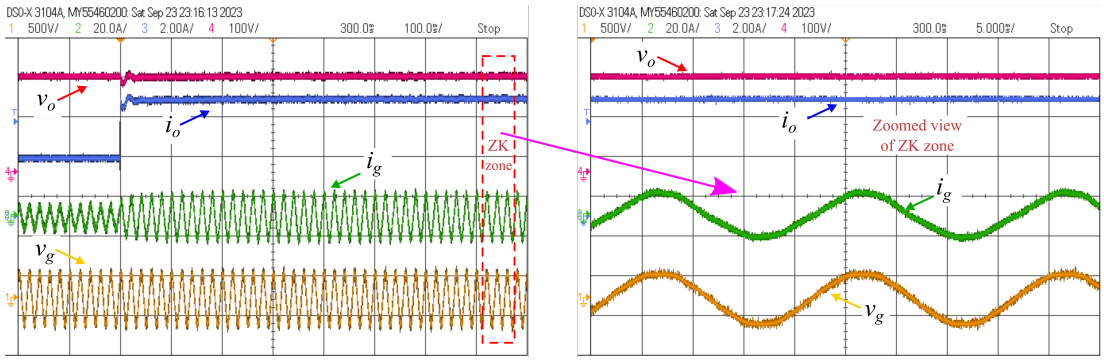
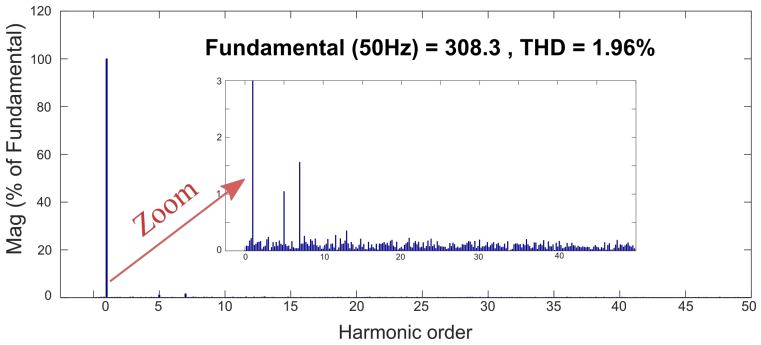


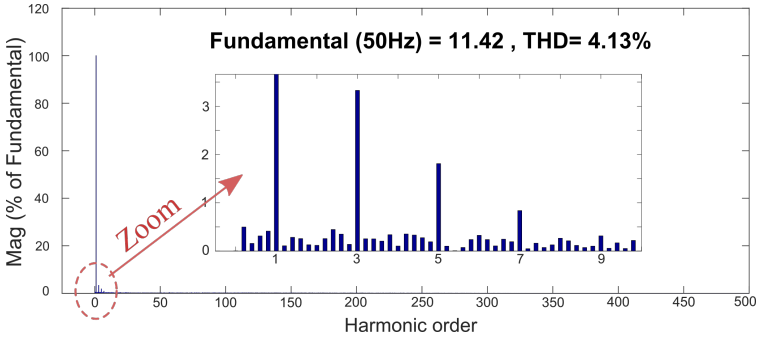
Figure 4.11: Experimental result showing v_g and i_g during load transient with zoomed view. Top trace: v_o (100 V/div), 2nd trace: i_o (2 A/div), 3rd trace: i_g (20 A/div), Bottom trace: v_g (500 V/div). Time:- (a) - 100 ms/div, zoomed view - 5 ms/div.

presentation with it. This was performed by applying the same 50% step increase in load as previously conducted. The corresponding results are illustrated in Figure 4.10. In the absence of feed-forward compensation, the overshoot/undershoot in MVDC voltages is approximately $4-6\%$ (Figure 4.10a). Conversely, with feed-forward compensation, a substantial reduction in the overshoot to approximately 1.5% is attained (Figure 4.10b). Effect of step load transient on grid current dynamics is shown in Fig. 4.11. The settling time for i_g is around 3 to 4 grid cycles. Throughout these transients, UPF operation still remains intact. The FFT plot of the grid voltage is depicted in Figure 4.12a, while Figure 4.12b shows the FFT plot of the grid current. At the deployment site, the THD of v_g was measured to be approximately 1.9%. After achieving voltage and power balance in the steady state, the THD of i_g was determined to be 4.13%, adhering to the IEEE 519-2014 standard.

The next set of experiments were carried out to showcase the output current regulation capability of the proposed control scheme. The functionality of the inner estimation based current loop was tested independently by deactivating the outer v_o voltage loop. Fig. 4.13 presents the experimental results for the current tracking performance. As the reference i_o^* was incremented from (5A $\rightarrow$ 6A $\rightarrow$ 7A) in steps, it is evident that i_o smoothly follows the changing set points. Since the load is resistive, v_o also increased correspondingly from (210V $\rightarrow$ 250V $\rightarrow$ 295V), resulting in a total voltage variation of approximately $\pm 15\%$.



(a) FFT plot of v_g.

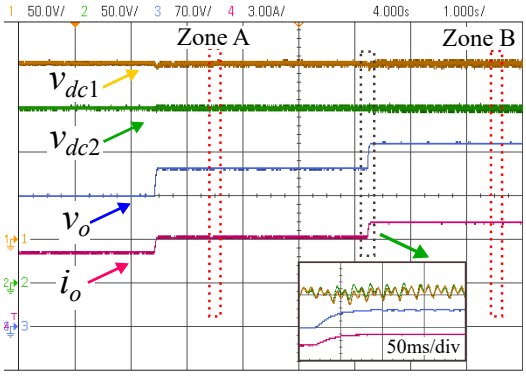


(b) FFT plot of i_g.

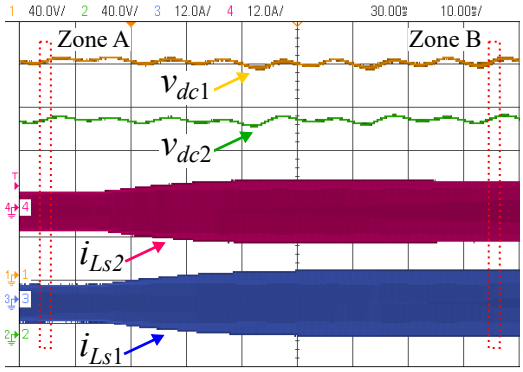
Figure 4.12: FFT Plot of grid voltage and current.

This is illustrated in Fig. 4.13a. The MVDC voltages v_{dc1} and v_{dc2} remain tightly regulated, as evident in Figure 4.13b. The operating modes of the two DABs change in response to the values of v_o as 215V - buck mode, 260V - unity gain mode and 295V - boost mode. Unity gain mode and boost mode are labeled as Zone A and Zone B respectively. Fig. 4.13c depicts the enlarged views of these zones, superimposing the oscilloscope reference for HF-link currents. It is apparent that i_{Ls1} and i_{Ls2} remain almost evenly distributed regardless of the mode of operation. This confirms the effectiveness of the proposed scheme in regulating output current while ensuring equal power sharing.

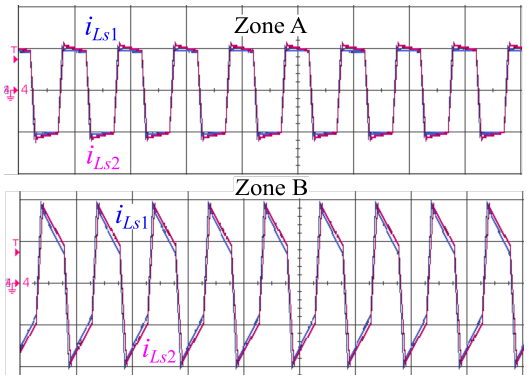
Another series of experiments were carried out to confirm the controlled zero power sharing capability (phase-shedding/plug-out operation) of the proposed control strategy. In this scenario, the current reference of one SST cell was promptly set to zero. The outcomes of these experiments are depicted in Fig. 4.14. This experiment was conducted with a lower



(a) step increase in i_o reference.



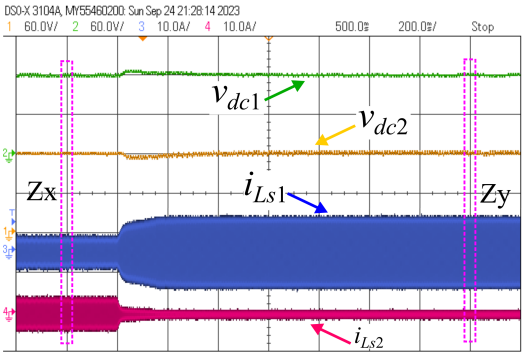
(b) Equal sharing of inductor currents.



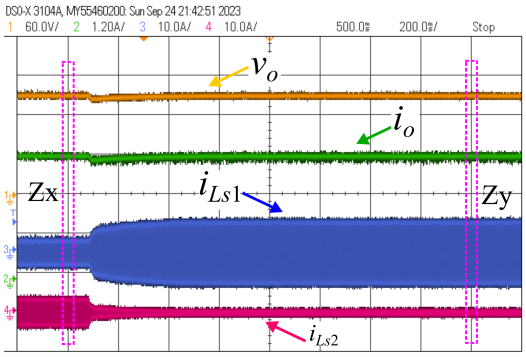
(c) i_{Ls1} and i_{Ls2} zoomed view.

Figure 4.13: Experimental results showing output current regulation. (a) Top trace: v_{dc1} (50 V/div), 2nd trace: v_{dc2} (50 V/div), 3rd trace: v_o (70 V/div), Bottom trace: i_o (3 A/div). (b) Top trace: v_{dc1} (40 V/div), 2nd trace: v_{dc2} (40 V/div), 3rd trace: i_{Ls2} (12 A/div), Bottom trace: i_{Ls1} (12 A/div). (c) Zoomed view of superimposed i_{Ls1} and i_{Ls2} (5 A/div). Time:- (a) 1 s/div, (b) 10 ms/div, (c) 50 μs/div.

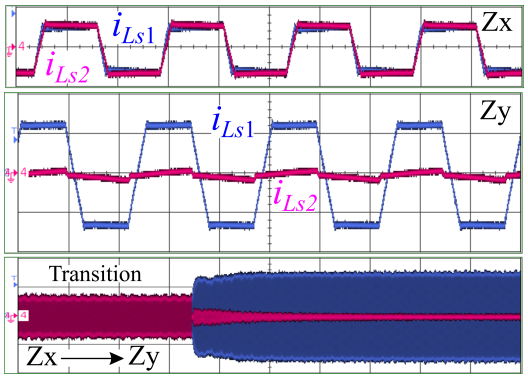
FEC modulation index due to hardware constraints imposed by the limited two number of SST cells and the current rating of the grid interfacing inductance (L_g) used during the experiments. The reduced modulation index also forced the MVDC and LVDC voltages to be operated at 125V and 160V respectively. Initially, the modulation index of both FEC cells was set approximately at 0.4. The outer v_o control loop produced identical i^*_{Ls1I} values for both SST cells. Subsequently, for cell 2, the activation input (act_2) was set to low. Consequently, the i_{Ls2} current reference was forced to zero. As a result, the H_{VO} controller adjusted i^*_{Ls1I} accordingly to maintain v_o and load power. Now all the active power transfers



(a) MVDCs during second cell phase-shedding.



(b) v_o and i_o during second cell phase-shedding.



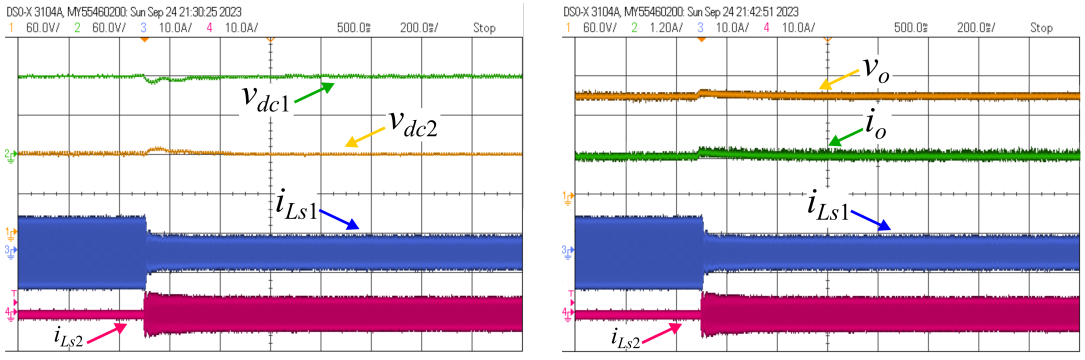
(c) i_{Ls1}, i_{Ls2}: Zoomed view and their transition.

Figure 4.14: Experimental results showing phase-shedding (plug-out) operation of cell 2. (a) Top trace: v_{dc1} (60 V/div), 2nd trace: v_{dc2} (60 V/div), 3rd trace: i_{Ls1} (10 A/div), Bottom trace: i_{Ls2} (10 A/div). (b) Top trace: v_o (60 V/div), 2nd trace: i_o (1.2 A/div), 3rd trace: i_{Ls1} (10 A/div), Bottom trace: i_{Ls2} (10 A/div). (c) Zoomed view of superimposed i_{Ls1} and i_{Ls2} (5 A/div). Time:- (a) 200 ms/div, (b) 200 ms/div, (c) Zx & Zy: 20 μs/div, Transition: 100 ms/div.

through cell 1, with no power being transferred by cell 2 in the steady state. Throughout this process, both MVDCs are regulated equally as given in Fig. 4.14a. The LVDC remains regulated while maintaining the same load power as prior to phase-shedding, as depicted in Figure 4.14b. It is evident that during the equal power distribution, the currents i_{Ls1} and i_{Ls2} are equal, corresponding to Zone X (Zx). In the phase-shedding mode, i_{Ls1} doubles, while i_{Ls2} becomes zero, corresponding to Zone Y (Zy) as shown in Fig. 4.14c. In the steady state, the FEC2 modulation index d_2 reaches 0.8, while d_1 is automatically reduced to zero by the H_{VBC} controller of CMFEC. In SST systems with a higher number of cells, the FEC

modulation duty will adjust by a factor of $[n/(n-1)]$, preventing the FECs from entering the over-modulation region. Thus, as illustrated, this approach allows for varying duty ratios in FEC modules within the modular SST, enabling the equal as well as controlled unequal and zero power sharing through its cells if necessary. This makes the power sharing to be more flexible. This functionality is highly beneficial for the controlled shutdown of a cell during periods of low load demand, enabling other cells to operate closer to their rated conditions. Throughout this period of reduced demand, the MVDC bus voltage in the deactivated cell remains consistently regulated. Consequently, when there is an increase in load demand, the previously deactivated cell can be swiftly reactivated to participate in power delivery, as the MVDC link capacitor is already precharged. The phase addition of cell 2 is depicted in Fig. 4.15, demonstrates the restoration of i_{Ls2} from zero to its rated value in less than 50 ms. Since the MVDC capacitors are already precharged, there is no need for an additional precharge circuit during phase-addition, facilitating a seamless and fast process.

Final experiment was conducted to verify the capability of monitoring the peak envelope of the DAB HF-link current. Utilizing observer-based estimation, the fundamen-

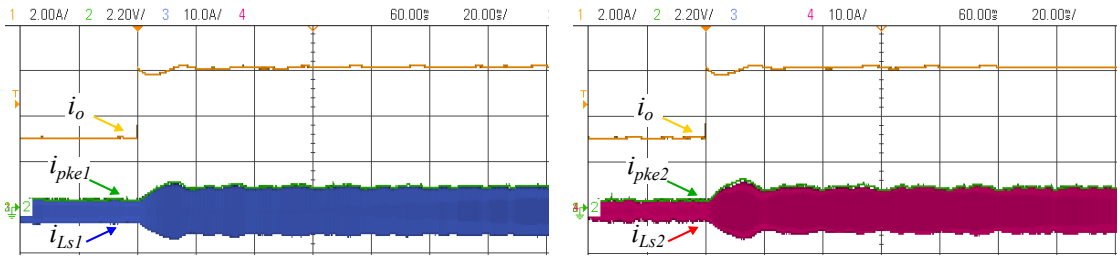


(a) MVDC voltages during phase-addition.

(b) v_o and i_o during phase-addition.

Figure 4.15: Experimental result showing phase-addition (plug-in) operation of cell 2. (a) Top trace: v_{dc1} (60 V/div), 2nd trace: v_{dc2} (60 V/div), 3rd trace: i_{Ls1} (10 A/div), Bottom trace: i_{Ls2} (10 A/div). (b) Top trace: v_o (60 V/div), 2nd trace: i_o (1.2 A/div), 3rd trace: i_{Ls1} (10 A/div), Bottom trace: i_{Ls2} (10 A/div). Time:- (a) 200 ms/div, (b) 200 ms/div.

tal harmonic $\langle i_{Lse1} \rangle_1$ and $\langle i_{Lse2} \rangle_1$ were estimated and subsequently used to determine the peaks of i_{Ls1} and i_{Ls2} represented as i_{pke1} and i_{pke2} respectively. During a 50% step increase in load, the tracking of peak current i_{Lsn} is illustrated in Fig. 4.16. It is evident that the estimated peak envelope closely follows the actual inductor current peak. This peak information can serve as an extra indicator for each DAB module to prevent it from experiencing over-current faults.



(a) Peak envelope monitoring of i_{Ls1} **(b)** Peak envelope monitoring of i_{Ls2}

Figure 4.16: Top trace of (a) & (b): i_o (2 A/div). 2nd Trace of (a): i_{pke1} and 2nd Trace of (b): i_{pke2} (2.2 V/div). Bottom Trace of (a): i_{Ls1} and Bottom Trace of (b): i_{Ls2} (10 A/div). Time:- 20 ms/div.

4.5.1 Impact of Computational Burden

In the proposed method, only the fundamental envelope of the inductor current is estimated, not the high-frequency inductor current itself. Since only the low-frequency average component is required for power balance, the computational burden is reduced. Furthermore, the inductances need not be estimated continuously. Once inductance estimation is done and updated in the observer block, the inductance estimation block can be deactivated. Once power balance is nearly achieved, all the FEC duty cycles will become almost equal $[d_1 \approx d_2 \approx d_3]$. Due to ageing, if the inductance value changes in the future, power imbalance would follow, and it will automatically reflect in the FEC duty cycles, making them unequal $[d_1 \neq d_2 \neq d_3]$. These FEC duty cycles can be used as an indicator of parametric uncertainty due to ageing. At this moment, the inductance estimation block can be

reactivated to estimate the inductance values again and update them in the observer block. Subsequently, power balance can be restored, further reducing the computational burden.

The control algorithm is implemented on the TMS320F2837xD LaunchPad, an affordable digital controller (approximately $35). In large-scale industrial mass production, costs would be significantly lower due to high production volume. Performance analysis during experiments shows that the code execution time for a two-cell SST (used in this work) with the proposed control method is $36\,\mu s$, while for a single SST cell, it is $29\,\mu s$. Notably, the processor used in this work is a single-core DSP, and the code is also not fully optimized. With advanced and powerful multi-core processors, such as quad-core DSPs, which are currently easily available in the market, the computational burden can be further minimized, making real-time implementation even easier. Additionally, the loop running time can be set as 2–3 times the ADC sampling time. This will not have a significant impact on bandwidth if the switching frequency of the converter is high. Yes, there will be a potential challenge of computational burden and high code execution time when scaling the proposed strategy to a large system. However, this challenge can be addressed using multi-core microprocessors.

4.5.2 Impact of Component Tolerances on Control Performance

In real-world converter design, the control stage, sensing stage, protection stage, and gate driver circuitry stage should all have component tolerances of less than $\pm 1\%$. Depending on the application, it can be as low as $\pm 0.1\%$ to further reduce the steady-state error. Apart from these stages, the major components of the power stage include semiconductor devices, capacitors, high-frequency as well as low-frequency magnetics, relays, circuit breakers, etc. Among these, the control performance is generally impacted by the tolerance of the capacitor and the leakage inductance value L_{sk}, as these are the energy-storing state variables of the system.

Variation in L_{sk} Leakage Inductance

$$p_{dabk} = \frac{N_{tk} v_o v_{dck}}{2 f_s} \frac{1}{L_{sk}} d_{\varphi k}(1 - d_{\varphi k}). \tag{4.27}$$

The power flow of the k^{th} DAB cell depends on the turns ratio N_{tk}, DAB output voltage v_o, DAB input voltage v_{dck}, DAB switching frequency f_s, DAB inductance L_{sk}, and DAB phase shift duty ratio $d_{\varphi k}$. Since the turns ratio and switching frequency are constant, and due to voltage balance control, v_o and v_{dcn} remain the same for all modular DABs. Hence, the power flow of the DAB is dependent only on L_{sk} and $d_{\varphi k}$. In this proposed control strategy, the real-time state estimation of L_{sk} (DAB inductance) effectively accounts for cell-to-cell tolerance variation. This is also experimentally validated by considering a $\pm 15\%$ variation.

Variation in Input C_k and Output C_o Capacitor

The power balance control will not be affected by cell capacitance deviation. Capacitance value variation only affects the ripple in the DC link capacitance voltage as given below.

$$\downarrow C_k \Longleftrightarrow \text{Ripple of } v_{dck} \uparrow \qquad\qquad \downarrow C_o \Longleftrightarrow \text{Ripple of } v_o \uparrow \tag{4.28}$$

The power balance control will also not be affected by different cell capacitance due to manufacturing or ageing. A change in capacitance value only alters the switching ripple and the 100 Hz second harmonic ripple in the voltages. However, the average DC value of v_o and v_{dck} does not change with cell capacitance deviation. Since the DC value remains the same, power balance control remains unaffected. It only influences the transient response of the system.

The state feedback gain matrix (k_e) in the observer block is designed using the pole placement method, positioning its pole ten times higher to minimize the error between v_o (actual measured state) and v_{oe} (estimated state). The k_e matrix nullifies the estimation

error in v_{oe} due to capacitance variations. Due to the variation of C_k and C_o, only transient performance parameters such as settling time and overshoot are affected, not the steady-state power and voltage balance control performance.

To address this, during the controller design process, a 20–30% variation in capacitor value from the nominal point should be considered, with sufficient phase margin for the worst-case plant transfer function. Furthermore, in practical applications, if the capacitance changes by 20%, its Equivalent Series Resistance (ESR) increases by a factor of two. At this point, the capacitor requires replacement. ESR serves as an indicator of capacitor degradation during health monitoring. A variation of more than 20% in electrolytic capacitance tolerance significantly affects the capacitor's lifetime, directly impacting the mission profile and the product warranty period.

4.6 Concluding Remarks

A high-bandwidth current sensorless flexible power sharing control strategy for modular ISOP SST is detailed in this chapter. The methodology revolves around estimating the active component of the fundamental harmonic of the HF-link inductor current, serving as the cornerstone for inner loop feedback in observer-based power balance control. This estimation technique also enables real-time monitoring of the inductor current peak envelope. This strategy facilitates controlled zero power sharing (phase-shedding) while regulating the MVDC voltages, obviating the need for additional MVDC link capacitor precharge circuit, making the whole process seamless. The control system is also reconfigurable for applications necessitating current regulation, all while maintaining power balance and MVDC voltage balance, owing to direct control handle over the active component of the fundamental current. The current sharing error is found within $\pm 4\%$ over a load power variation range of 30% to full load, even without the use of high-bandwidth current sensors. This was achieved despite a 15% parametric variation in HF-link inductances from

their rated values. All the aforementioned features of the proposed control scheme have been validated through experiments.

The effectiveness of the proposed sensorless power-sharing strategy is inherently dependent on precise parameter identification, particularly the estimation of HF-link inductance L_s. This challenge has been addressed in this work through a proposed online parameter identification scheme, which has been experimentally validated. The basis of the inductance estimation scheme lies in equating the active component of the input current of the DAB module with the active component of the output current of its series-connected FEC module, forming the foundation of the modular SST inductance estimation approach. The results confirm that the power-sharing error remains within 4% using this approach. To further enhance the robustness of parameter estimation, advanced techniques such as Model Predictive Control, Extended Kalman Filters, Sliding Mode Observers, and AI-based estimators can be explored. Since robust parameter identification is a broad and complex topic, an in-depth investigation of these advanced methodologies will be pursued as part of future research work.

Chapter 5

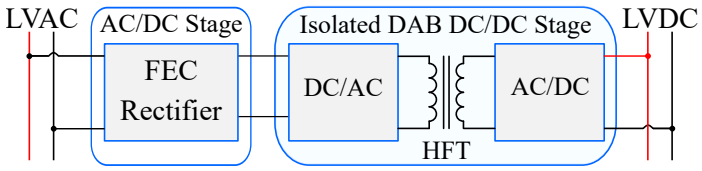
Estimation Based Flexible Power Sharing Control of IPOP SST

In this chapter, the voltage balance and flexible power sharing control strategy for another important modular structure, the input-parallel-output-parallel (IPOP) configuration, have been detailed. In Chapter 4, the input-series-output-parallel (ISOP) configuration is discussed, where the FECs of SST are connected in series for input side high voltage applications. On the other hand, for input side high current applications, the FECs of the SST need to be connected in parallel, forming the IPOP configuration. This chapter focuses on the requirements of the IPOP configuration, emphasizing its voltage balance and flexible power sharing control technique. A key challenge addressed here is achieving UPF operation for multiple parallel units on the grid side using only one current sensor. Finally, experimental results are presented for the validation.

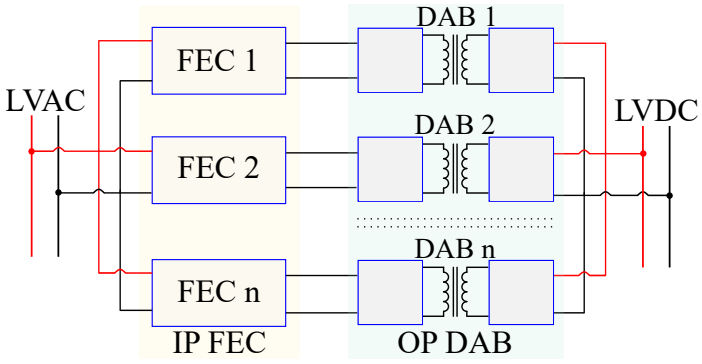
5.1 Requirement of an IPOP Configuration

As global renewable energy penetration continues to rise, there has been increasing interest in hybrid microgrids and low-voltage distribution systems. These systems can effectively integrate diverse elements such as distributed energy resources, electric vehicle

charging stations, and energy storage systems (ESS). To integrate a DC distribution system with a low-voltage AC (LVAC) grid, an isolated bidirectional AC-DC converter is required. The two-stage isolated AC-DC converter topology is a favoured solution due to its weak line-load dynamic coupling and excellent disturbance rejection capabilities. The two-stage topology serves as the foundational block of the modular ISOP SST configuration, which was the topology of focus in the Chapter 4. Similarly, the two-stage isolated AC-DC converter also forms the building block of the input-parallel-output-parallel (IPOP) AC-DC system, which is the topology of focus in this chapter. The block diagram of isolated two stage LVAC-LVDC conversion system is shown in Fig.5.1. The IPOP configuration offers benefits such as: enhanced reliability, simplified maintenance, design flexibility, ease of system reconfiguration and seamless phase-shedding/phase-adding operations. It holds significant potential for interfacing loads requiring low-voltage-high-current, with the utility grid. The IPOP system emerges as a compelling solution to bolster the overall power capability of hybrid ESS [73, 74]. In Chapter 4, the HBW current-sensorless voltage and power balance control strategy of ISOP SST to counteract imbalances stemming from mis-



(a) Single module FEC & DAB.



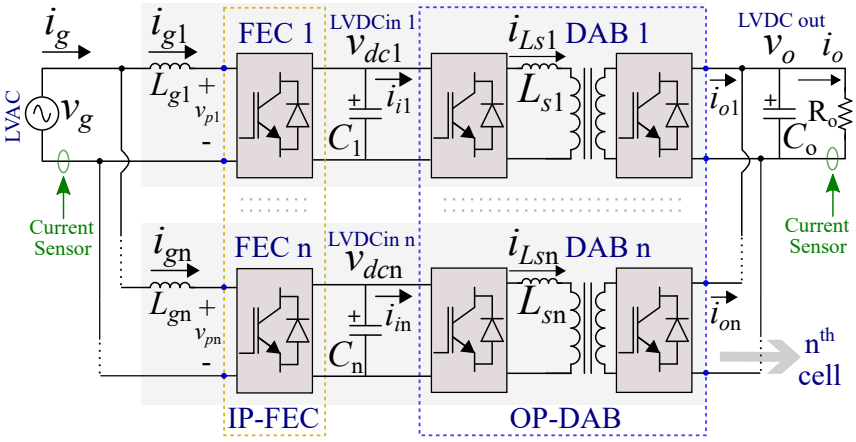
(b) Modular IP-FEC & modular OP-DAB.

Figure 5.1: Block diagram of isolated two stage LVAC-LVDC conversion system.

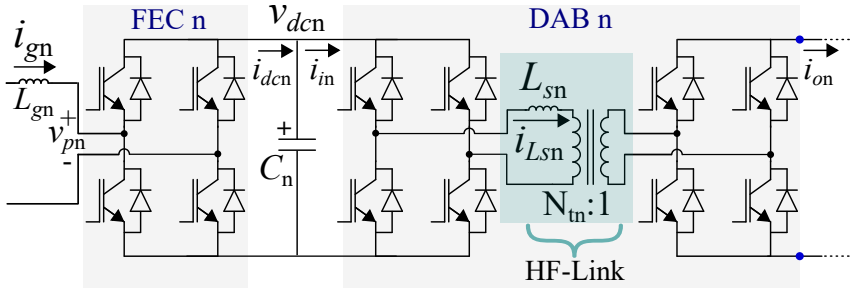
match in HF-link inductance is detailed. However, there have been negligible known efforts to investigate the IPOP AC-DC system and its power balance control strategy without the dependence on cell-to-cell current sensors or HBW current sensors. Next, an overview of previous literature is provided, highlighting where the proposed control stands out.

5.2 Reported Control Schemes and the Proposed Strategy

Sensorless control strategies for IPOP DC-DC configurations has been studied extensively, with achieving cell-to-cell power balance being a key focus in numerous studies [75, 76, 77, 78, 79, 80]. In [75], a common duty ratio control scheme is introduced, aiming to remove the need for current sensors. Consequently, the imbalance in power sharing grows with greater parametric uncertainty. Meanwhile, [76, 77, 78] present a current sensor-



(a) Modular IPOP configuration based on IPFEC & OPDAB.



(b) Circuit diagram of n^{th} cell.

Figure 5.2: Circuit diagram of modular IPFEC-OPDAB topology.

less power balance control strategy for IPOP-DAB, which is based on perturbation of the phase-shift-duty ratio. These approaches are based on a reduced-order dynamic model of DAB that excludes the HF-link current (i_{Ls}) as a state variable. In [79], sensorless current discrepancy mitigation technique is proposed using coupled inductor. However, this method leads to increased complexity in magnetic core design as the number of cells increases and it necessitates an additional passive selector for phase-shedding/adding operations. In certain cases, the IPOP DC-DC conversion system is connected to the grid via a non-modular single module AC-DC converter, with its primary aim being to draw unity power factor (UPF) current from the grid [73, 80]. Here in this chapter, the topology of focus is IPOP AC-DC converter, which is fully modular. The first AC-DC conversion stage is input-parallel-front-end-converter (IPFEC) and the second DC-DC conversion stage is output-parallel-dual-active-bridge (OPDAB), where both the stages are modular. The detailed circuit diagram representing this configuration is depicted in Fig. 5.2. The current sensorless control schemes mentioned above are specifically designed for IPOP DC-DC configurations. They cannot be directly adapted for controlling IPOP AC-DC converter. Therefore, the aim is to devise a current sensorless flexible power sharing control scheme for IPOP AC-DC converter, a topic that has not been explored in previous literature. The overall control objectives of the proposed strategy are,

1. Achieving UPF operation for the grid current (i_g).

2. Ensuring UPF operation for all parallel branch currents (i_{g1}, i_{g2}, ..., and i_{gn}).

3. Maintaining voltage balance across the FEC-output/DAB-input LVDCin voltages ($v_{dc1} = v_{dc2} = ... = v_{dcn}$).

4. Regulating the total summation of LVDCin voltages.

5. Ensuring equal power distribution among the IPOP cells.

6. Achieving flexible power sharing during contingency situations.

7. Regulating the LVDC output voltage (v_o).

In the subsequent sections of this chapter, the IPFEC stage voltage balance control, the OPDAB stage flexible power sharing control is discussed.

5.3 IPFEC Stage Voltage Balance Control

The objective of LVDC input (LVDCin) voltage balancing is accomplished in this IPFEC stage control. Ensuring that all parallel branch currents align in phase with v_g holds equal importance to ensuring that i_g itself is in phase with it. Otherwise, it could result in an unequal distribution of RMS currents among the parallel IPFEC modules, potentially leading to operational failure due to non-uniform device stress. A single low bandwidth current sensor is installed at the grid side to measure i_g. The major challenge lies in keeping all parallel branch currents in UPF with i_g, without measuring them individually.

Initially an orthogonal phase is generated using the second-order generalized integrator (SOGI) for vector control. The resulting orthogonal axes, α and β, are subsequently transformed into the rotating dq reference frame. Alignment of the grid voltage along the d-axis is achieved using PLL. Here, the d-axis and q-axis components signify the active and reactive components respectively. Representing the grid angular frequency as ω_g, the pole voltage of the n^{th} FEC module (v_{pn}) can be expressed as,

$$v_{pn} = v_g - j\omega_g L_{gn} i_{gn} = v_g - j\omega_g L_{gn}(i_{gdn} + j i_{gqn}). \tag{5.1}$$

$$v_{pn} = d_n v_{dcn} = (d_{dn} + j d_{qn}) v_{dcn}. \tag{5.2}$$

Here, L_{gn} and d_n denotes the grid interfacing inductance and modulation-duty ratio of n^{th} FEC respectively. Equating (5.1) with (5.2) and rearranging real and imaginary terms, the

following relations are arrived at.

$$d_{dn}v_{dcn} = v_g + \omega_g L_{gn} i_{gqn}. \tag{5.3}$$

$$d_{qn}v_{dcn} = -\omega_g L_{gn} i_{gdn}. \tag{5.4}$$

To achieve unity power factor (UPF) operation across all parallel-connected FEC modules, the reactive component i_{gqn} must be zero. Thus, setting this variable to zero results in,

$$d_{dn} = v_g / v_{dcn}, \tag{5.5}$$

$$d_{qn} = -(\omega_g / v_{dcn}) L_{gn} i_{gdn}. \tag{5.6}$$

From equation (5.5), it is evident that the equality of d_{dn}, representing the active component of duty ratio, among all FEC modules is a prerequisite for achieving LVDC voltage balance ($(v_{dc1} = v_{dc2} = ... = v_{dcn})$). Therefore, the necessary condition is,

$$d_{d1} = d_{d2} = ... = d_{dn}. \tag{5.7}$$

Ignoring the switching ripple component, the output current of the n^{th} FEC (i_{dcn}), its active component (i_{in}) and i_{gn} are interrelated as,

$$i_{dcn} = d_n i_{gn} = (d_{dn} + j d_{qn}) i_{gdn}, \tag{5.8}$$

$$i_{in} = d_{dn} i_{gdn}. \tag{5.9}$$

After substituting (5.6) into (5.9), the expression (5.10) is derived. Equality of i_{in} across all cells is achieved through DAB stage control, which is outlined in the subsequent section. Once this condition is attained, it can be deduced from (5.6) and (5.10), that the control

variable for compensating the mismatch in grid-side inductance L_{gn} is d_{qn}. This is where it was found to be completely different from modular ISOP SST control, where modification of the active component of duty cycle is utilized to achieve the control objective.

$$i_{in} = -\left[\frac{v_{dcn} d_{dn}}{\omega_g}\right] \frac{d_{qn}}{L_{gn}} \quad \Longrightarrow \quad d_{qn} \propto i_{in} L_{gn}. \tag{5.10}$$

Hence, the control scheme of the IPFEC stage is based on (5.6) to (5.10), where d_{dn} is maintained constant and d_{qn} is modified to achieve voltage balance. Carrier interleaved sine triangle unipolar PWM technique is applied for generating gating signals. The overall

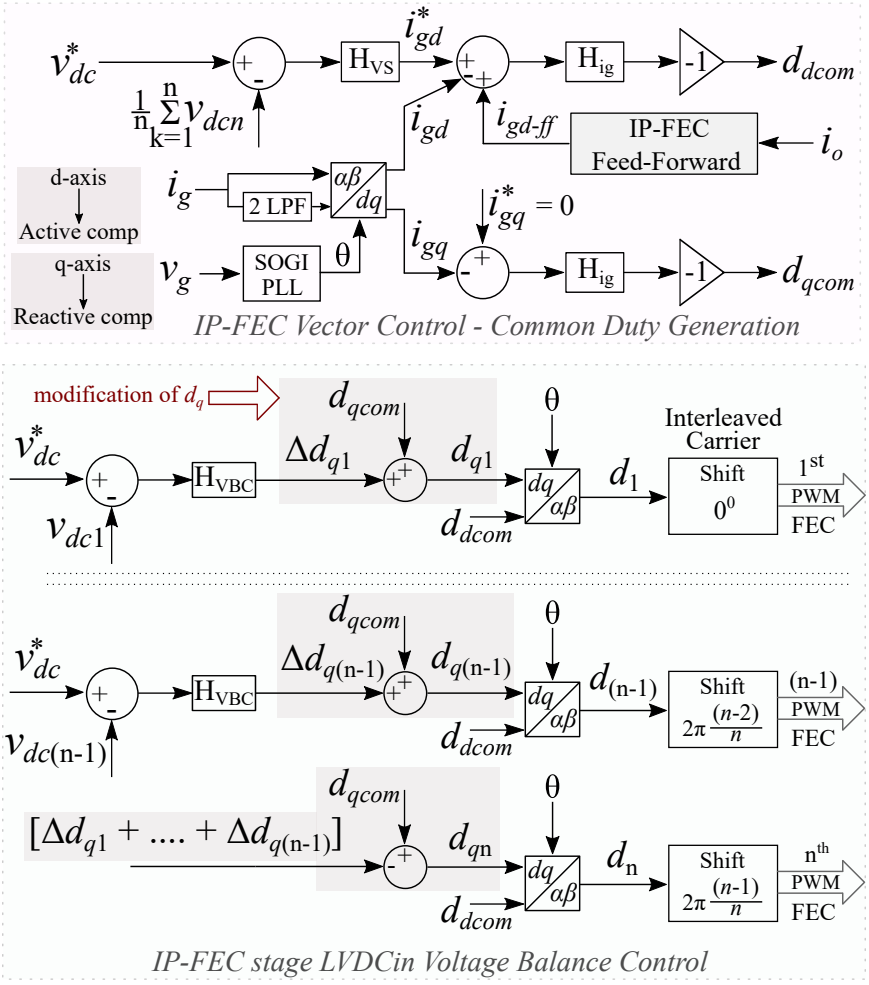


Figure 5.3: Proposed control scheme for the IPFEC stage.

control scheme is depicted in Fig. 5.3. Employing vector control approach, both the active component (d_{dcom}) and reactive component (d_{qcom}) of the common duty (d_{com}) are generated. To attain the objective of voltage balancing, the common reactive component (d_{qcom}) is added to the output of voltage balance controller (H_{VBC}) to derive the modified d_{qn} for n^{th} FEC. This modification of the reactive component d_{qn} ensures both voltage balance and UPF operation across all FEC modules of IPFEC with this proposed control methodology.

The active component d_{dn} is maintained uniform across all FECs as d_{dcom}, while d_{qcom} represents the average of the reactive components of all FECs, therefore making sum of all Δd_{qn} equal to zero under voltage balance,

$$d_{qcom} = \frac{1}{n}\Big[\sum_{k=1}^{n} d_{qk}\Big] \qquad \text{and} \qquad \sum_{k=1}^{n} \Delta d_{qk} = 0. \tag{5.11}$$

A feed-forward term is incorporated into the inner current loop of IP-FEC control to enhance performance during load transients. This term, denoted as i_{gd-ff}, is defined in (5.12), where D_{dcom} represents the nominal active component of the common duty ratio:

$$i_{gd-ff} = \frac{1}{N_{tn} D_{dcom}} i_o. \tag{5.12}$$

5.4 OPDAB Stage Power Balance Control

The power transfer (p_n) in the n^{th} DAB cell with single phase shift (SPS) modulation is given as,

$$p_n = i_{in} v_{dcn} = \frac{N_{tn} v_o v_{dcn}}{2 f_s} \frac{1}{L_{sn}} d_{\varphi n}(1 - d_{\varphi n}). \tag{5.13}$$

Here, f_s represents the switching frequency of DAB and $d_{\varphi n}$ denotes the phase shift duty ratio. The power flow is directly influenced by the HF-link inductance (L_s) and turns ratio (N_t), with variations in these parameters between cells leading to unequal active power distribution. By equating (5.10) and (5.13), the expression in (5.14) is derived, serving as

the foundation for the overall two-stage control approach in this research work.

$$-\frac{2f_s d_{dn} v_{dcn}}{\omega_g v_o} = \underbrace{\left[\frac{L_{gn}}{d_{qn}}\right]}_{\text{IPFEC-cmpn}} \underbrace{\left[\frac{d_{\varphi n}(1-d_{\varphi n})}{L_{sn}/N_{tn}}\right]}_{\text{OPDAB-cmpn}}. \tag{5.14}$$

Compensation for the cell-to-cell variation of L_{gn} is achieved through the modification of d_{qn} in the IPFEC stage compensation (IPFEC-cmpn), as discussed in the preceding section. The variation in (L_{sn}/N_{tn}) values among cells can be addressed by modifying $d_{\varphi n}$ in the OPDAB stage compensation (OPDAB-cmpn) to attain power balance. Here, the ratio of HF-link parameters (L_{sn}/N_{tn}) is represented as λ_n.

In this proposed scheme the control objectives are met through the estimation and subsequent control of the fundamental component of i_{Ls}. The central control structure for the OPDAB stage remains same as the observer based power balance control of modular DAB, which is discussed elaborately in Chapter 4. The block diagram of proposed estimation based flexible power sharing control scheme is reproduced and illustrated in Fig. 5.4. It is necessary to update the values of HF-link inductance (L_{sn}) in the corresponding state observer blocks after estimation. The methodology for estimating L_{sn} is discussed subsequently.

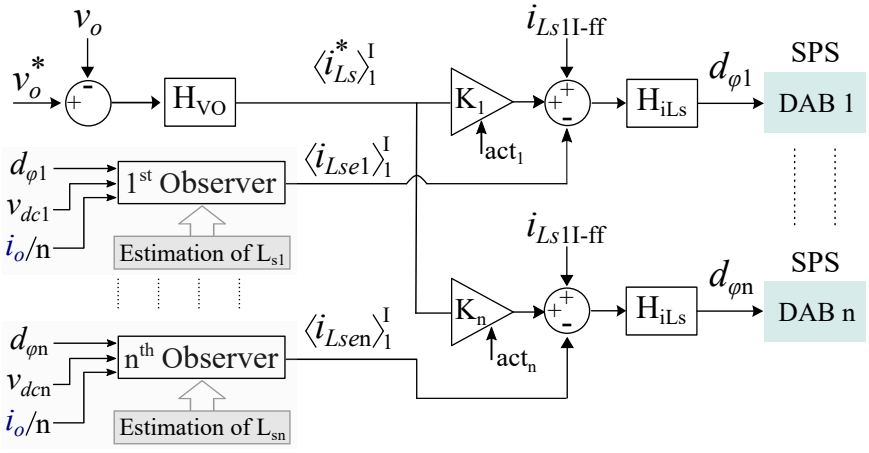


Figure 5.4: Proposed flexible power sharing control scheme for the OPDAB stage.

5.4.1 HF-Link Parameter Estimation

The HF-link parameter estimation techniques are documented in [61, 72, 81]. However, these methods are not suitable for this particular IPOP configuration. The parameter estimation technique using the inner loop fundamental current perturbation (FCP) is presented here for the IPFEC-OPDAB topology. This technique is implemented only after voltage balance is attained in the IPFEC stage. Initially, the FCP scheme is explained with an example focusing on two cell IPFEC-OPDAB setup. Later, its extension to scenarios with n number of cells is discussed. Various stages of the FCP scheme are detailed below.

Stage of Common Phase-Shift Duty Ratio (CPSD)

In the IPFEC stage, the voltage balance control ensures $v_{dc1} = v_{dc2} = v_{dc}$. The subsequent goal is to equalize the input current of DAB module (i_{in}) to meet the power balance objective. Different DAB modules may have distinct λ_n values, which are unknown initially. During the design process of the observer block for each DAB, it is assumed that the inductance value is same as the nominal or nameplate rating, that is, $\lambda_1 = \lambda_2 = \lambda_{nom}$. As a result, the H_{iLs} inner current controllers produce identical control inputs for each DAB, that is $d_{\varphi 1} = d_{\varphi 2} = d_{\varphi c}$. Consequently, in this stage the phase-shift duty ratio of each DAB module is common. Hence, there will be no power balance. The expressions for the input currents of DAB1 (i_{i1}) and DAB2 (i_{i2}) are provided in equations (5.15) and (5.16), respectively, where, $k = v_o/2f_s$.

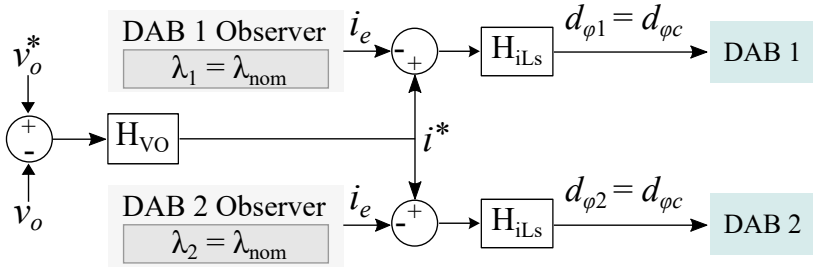
$$i_{i1} = \frac{N_{t1} v_o}{2f_s} \frac{d_{\varphi 1}(1 - d_{\varphi 1})}{L_{s1}} = k \frac{d_{\varphi c}(1 - d_{\varphi c})}{\lambda_1}. \tag{5.15}$$

$$i_{i2} = \frac{N_{t2} v_o}{2f_s} \frac{d_{\varphi 2}(1 - d_{\varphi 2})}{L_{s2}} = k \frac{d_{\varphi c}(1 - d_{\varphi c})}{\lambda_2}. \tag{5.16}$$

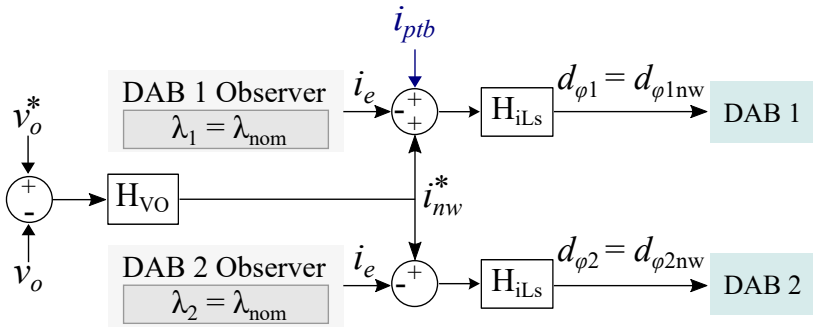
The total input power is given in (5.17). The inner current reference generated by H_{VO}

is symbolised as i^* instead of $\langle i^*_{Ls} \rangle^I_1$ for simplicity. CPSD stage is shown in Fig. 5.5a.

$$p_{in} = (i_{i1} + i_{i2})v_{dc} = kv_{dc}d_{\varphi c}(1 - d_{\varphi c})\Big[\frac{1}{\lambda_1} + \frac{1}{\lambda_2}\Big]. \tag{5.17}$$



(a) Stage of common phase-shift duty ratio.



(b) Stage of current perturbation in DAB1.

Figure 5.5: FCP strategy for 2 cell IPFEC-OPDAB.

Stage of Fundamental Current Perturbation (FCP)

In this phase, a small current perturbation (i_{ptb}) is introduced solely into the inner loop of DAB1. As the output voltage v_o remains regulated, the power supplied to the load remains constant during this process. Following the addition of i_{ptb}, the outer H_{VO} controller generates a new current reference i^*_{nw}. The observer blocks of both DABs, which are designed for $\lambda_1 = \lambda_2$ still estimate same the i_e. Consequently, the phase-shift duty ratios $d_{\varphi 1}$ and $d_{\varphi 2}$ changes from the common $d_{\varphi c}$ to $d_{\varphi 1nw}$ and $d_{\varphi 2nw}$, respectively. This stage of FCP is depicted in Fig. 5.5b. The input currents of DAB1 and DAB2 shift to new operating points i_{i1nw} and i_{i2nw}, respectively, as given in (5.18) and (5.19). The total input power in steady

state following the perturbation introduction is expressed in (5.20).

$$i_{i1nw} = \frac{N_{t1} v_o}{2 f_s} \frac{d_{\varphi 1}(1 - d_{\varphi 1})}{L_{s1}} = k \frac{d_{\varphi 1nw}(1 - d_{\varphi 1nw})}{\lambda_1}. \tag{5.18}$$

$$i_{i2nw} = \frac{N_{t2} v_o}{2 f_s} \frac{d_{\varphi 2}(1 - d_{\varphi 2})}{L_{s2}} = k \frac{d_{\varphi 2nw}(1 - d_{\varphi 2nw})}{\lambda_2}. \tag{5.19}$$

$$p_{in} = k v_{dc} \Big[\frac{d_{\varphi 1nw}(1 - d_{\varphi 1nw})}{\lambda_1} + \frac{d_{\varphi 2nw}(1 - d_{\varphi 2nw})}{\lambda_2} \Big]. \tag{5.20}$$

Stage of Parameter Estimation and Updation

The value of the HF-link parameter is estimated and refreshed in the observer blocks during this stage. The total power transfer remains constant, given that v_o is consistently regulated by the H_{VO} controller and the load resistance remains unchanged. Equating (5.17) with (5.20), the expression in (5.21) is derived, which calculates the ratio of HF-link parameters.

$$\frac{\lambda_2}{\lambda_1} = -\Big[\frac{d_{\varphi c}(1 - d_{\varphi c}) - d_{\varphi 2nw}(1 - d_{\varphi 2nw})}{d_{\varphi c}(1 - d_{\varphi c}) - d_{\varphi 1nw}(1 - d_{\varphi 1nw})} \Big] = f_1. \tag{5.21}$$

From the IPFEC stage, the expression for total input power is derived as in (5.22) and equating (5.17) with (5.22), the expression (5.23) is derived.

$$p_{in} = (i_{i1} + i_{i2}) v_{dc} = 0.5 (i_{gd} d_d v_{dc}), \tag{5.22}$$

$$\Big[\frac{1}{\lambda_1} + \frac{1}{\lambda_2} \Big] = \frac{i_{gd} d_d f_s}{v_o d_{\varphi c}(1 - d_{\varphi c})} = f_2. \tag{5.23}$$

Subsequently, using (5.21) and (5.23) the actual values of λ_1 and λ_2 can be calculated as

$$\lambda_2 = \Big[1 + f_1 \Big] / f_2 \qquad \text{and} \qquad \lambda_1 = \lambda_2 / f_1. \tag{5.24}$$

Once the estimates for λ_1 and λ_2 are obtained, they are then updated in the state observer

blocks of DAB1 and DAB2 respectively. The H_{iLs} controller operates to minimize the current error in each loop, consequently achieving power balance by the end of this stage.

Extension to n Cells Scenario

The procedure for estimating the HF-link parameters in an n-cell configuration follows a similar approach to that of the 2-cell case. However, only two cells are involved in the FCP stage at any given time. For the remaining cells, only their inner current loop remains active, with the outer voltage loop deactivated and the current reference fixed at i^* as obtained from the preceding CPSD stage. This configuration is depicted in Fig. 5.6. DAB1 is selected as the master module, and during the FCP stage, both DAB1 and DABn participate, with i_{ptb} added to DAB1 to determine the ratio λ_n/λ_1, as outlined in (5.25). Similarly, the ratios λ_2/λ_1, ..., $\lambda_{(n-1)}/\lambda_1$ can be sequentially calculated.

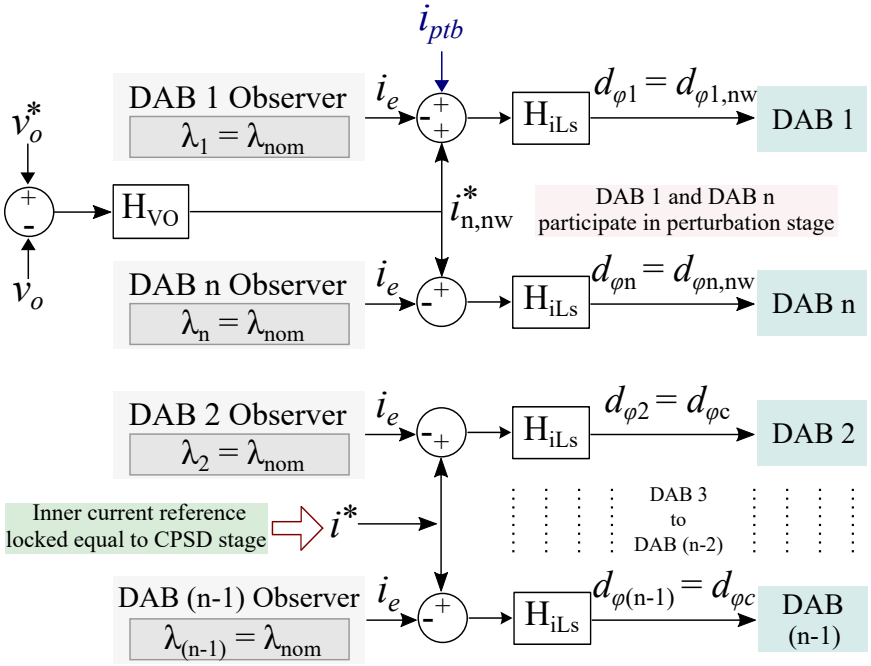


Figure 5.6: Stage of FCP between DAB1 and DABn.

$$\frac{\lambda_n}{\lambda_1} = -\left[\frac{d_{\varphi c}(1-d_{\varphi c}) - d_{\varphi n,nw}(1-d_{\varphi n,nw})}{d_{\varphi c}(1-d_{\varphi c}) - d_{\varphi 1,nw}(1-d_{\varphi 1,nw})}\right]. \tag{5.25}$$

Expression in (5.26) can be derived from the CPSD stage of all n DAB modules. Solving the λ_2/λ_1, ..., λ_n/λ_1 ratios and (5.26), the HF-link parameter values can be estimated.

$$\sum_{k=1}^{n} \frac{1}{\lambda_k} = \frac{i_{gd} d_d f_s}{v_o d_{\varphi c}(1 - d_{\varphi c})}. \tag{5.26}$$

5.4.2 Step by Step Implementation Procedure

A flowchart summarizing the step-by-step working procedure of the proposed scheme is depicted in Fig. 5.7. Once the objective of both voltage and power balance is achieved, the reactive component of the FEC modulation duty cycle d_{qn} will still differ across the cells due to variations in the value of L_g on the grid side as indicated by the expression in (5.10). Consequently, the modulation duty cycles of FECs become unequal in the steady state ($d_1 \neq d_2 \neq ... \neq d_n$). The only scenario in which the modulation duty cycles become equal is when all L_g values are exactly the same across cells, which is highly unlikely.

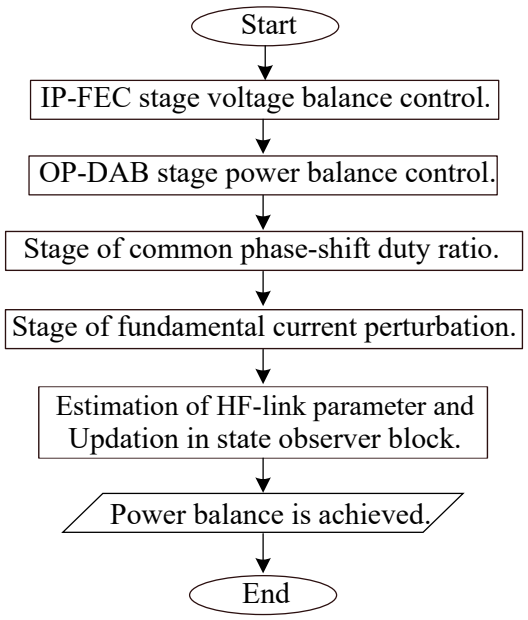


Figure 5.7: Flowchart showing implementation steps of the control scheme.

5.5 Results and Discussion

Experimental validation of the proposed control strategy for the IPFEC-OPDAB converter was conducted using a scaled-down hardware prototype with a power rating of 1.4 kW and comprising 2 cells. This setup is depicted in Fig. 5.8. The system parameters are listed in Table 5.1. Only two low-bandwidth current sensors with a bandwidth of 200 kHz were used to measure the currents i_g and i_o. Digital control was implemented using a TMS320F28377S DSP micro-controller and a SPARTAN-6 FPGA.

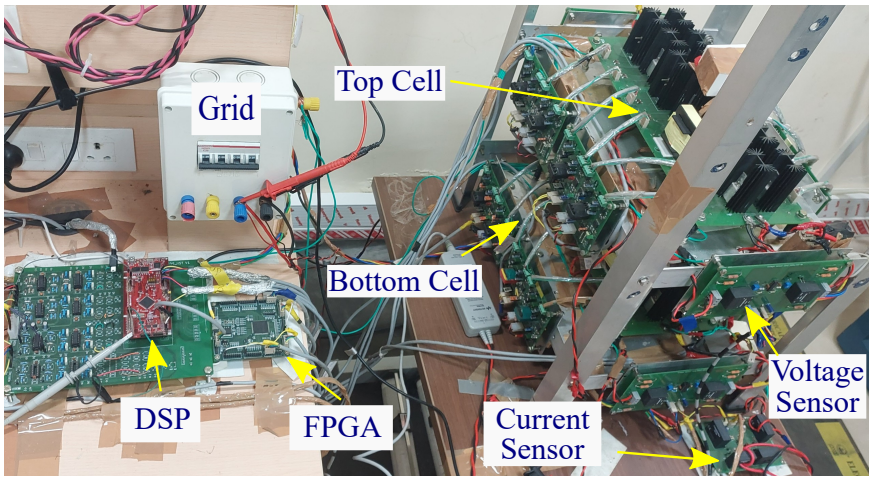
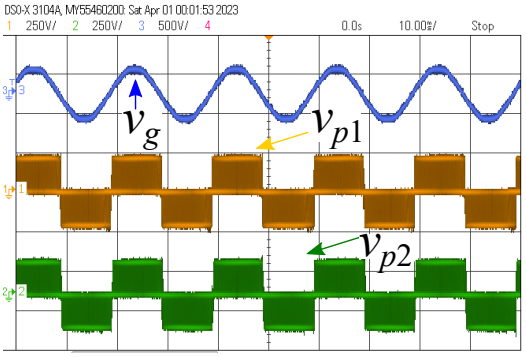


Figure 5.8: Experimental Prototype.

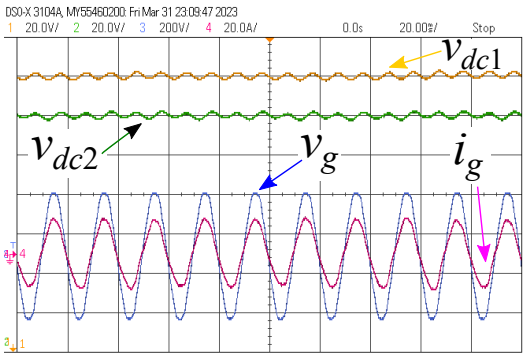
The HF-link inductances of the two DAB modules were intentionally chosen to have significantly different values: $L_{s1} = 128\mu H$ and $L_{s2} = 178\mu H$, introducing a parametric variation of $\pm 15\%$. Both the DABs were designed with the transformers having a turns ratio value of 0.8. Similarly, the two grid interfacing inductances L_{g1} and L_{g2} were chosen as 4 mH and 5.25 mH, respectively, with approximately $\pm 15\%$ parametric variation. Initially, the experiment focused on validating the voltage balance control of the IPFEC. At this stage, the control scheme operates under the assumption of nominal/nameplate HF-link parameter values. The experimental outcomes corresponding to this are illustrated in Fig. 5.9. Due to unipolar PWM, the pole voltages v_{p1} and v_{p2}, exhibit three levels (+200 V, 0 V,

Table 5.1: System Parameters

Parameter	Symbol	Value
DAB 1, 2 inductance	L_{s1}, L_{s2}	128, 178 μH
Nominal DAB inductance	L_{snom}	150 μH
LVDCout Capacitance	C_o	330 μF
LVDCin 1, 2 Capacitance	C_1, C_2	2, 2.2 mF
DAB Switching frequency	f_s	20 kHz
FEC Switching frequency	f_{FEC}	4 kHz
HF link turns ratio	N_{t1}, N_{t2}	0.8
Input LVDC voltage	V_{dcn}	200 V
Load side LVDC voltage	V_o	240 V
Grid input voltage (RMS)	v_g	125 V, 50 Hz
Rated grid side inductance	L_{g1}, L_{g2}	4, 5.25 mH
Total power	P_t	1.4 kW



(a) Pole voltages.

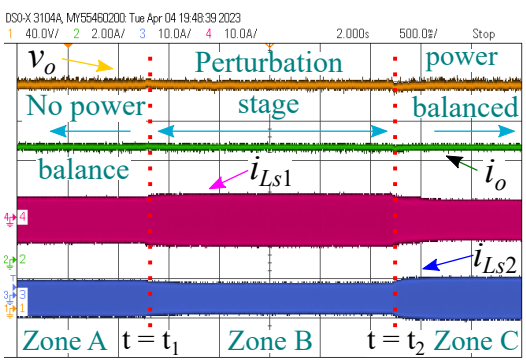


(b) Grid side UPF & voltage balance.

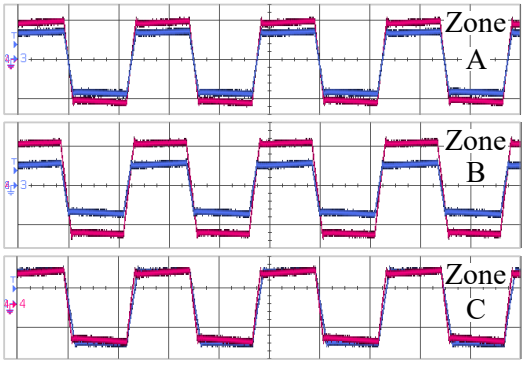
Figure 5.9: Experimental results showing voltage balance control of IP-FEC. (a) Top trace: v_g (500 V/div), 2nd trace: v_{p1} (250 V/div), Bottom trace: v_{p2} (250 V/div). (b) Top trace: v_{dc1} (20 V/div), 2nd trace: v_{dc2} (20 V/div), Bottom trace: v_g (200 V/div) and i_g (20 A/div). Time:- (a) 10 ms/div, (b) 20 ms/div.

-200 V), as illustrated in Fig. 5.9a. In the steady state, the two LVDCin voltages v_{dc1} and v_{dc2} are balanced with an equal value of 200 V. The peak-to-peak voltage ripple in v_{dc1} and v_{dc2} is approximately 8 V, predominantly comprising a dominant 100 Hz second harmonic ripple. These observations validate the effectiveness of the voltage balance control of the IPFEC, even with the presence of unequal inductances in both the DAB stage and the grid interfacing side.

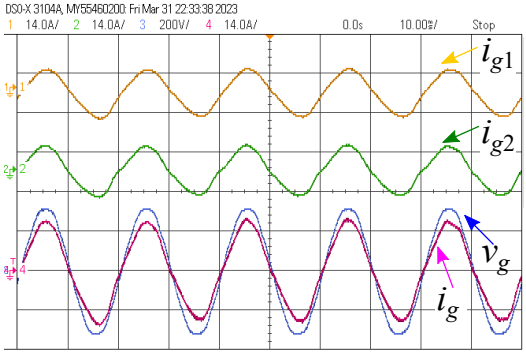
The subsequent series of experiments aimed to assess the effectiveness of the proposed power balance control strategy. Fig.5.10 depicts the experimental outcomes. Initially assuming identical HF-link inductance values across all cells, resulted in the generation of a common $d_{\varphi c}$ = 0.1627, indicating absence of power balance. Notably, the HF-link currents i_{Ls1} and i_{Ls2} exhibited inequality, with i_{Ls1} greater than i_{Ls2}. This is in line with expectations, due to the smaller actual inductance value of L_{s1} compared to L_{s2}. Moreover, $i_{Ls1,rms}$ and $i_{Ls2,rms}$ values were observed to be approximately 114.31% and 85.69% re-



(a) Current perturbation addition at $t = t_1$.



(b) i_{Ls1} and i_{Ls2} zoomed view in zones.



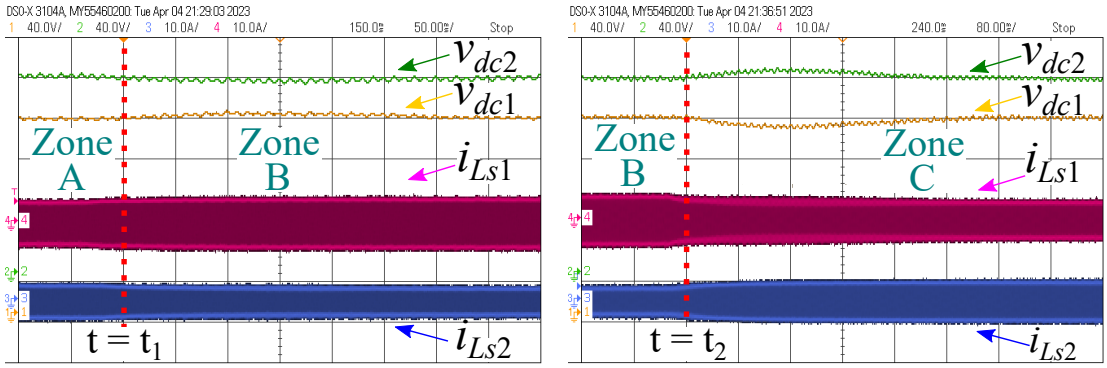
(c) Balanced IP-FEC input currents at steady state.

Figure 5.10: Experimental results showing fundamental current perturbation based power balance control. (a) Top trace: v_o (40 V/div), 2nd trace: i_o (2 A/div), 3rd trace: i_{Ls1} (10 A/div), Bottom trace: i_{Ls2} (10 A/div). (b) Zoomed view of i_{Ls1} and i_{Ls2} shown in (a) with their oscilloscope references superimposed. Upper trace: Zone A of (a), Middle trace: Zone B of (a), Bottom trace: Zone C of (a). (c) Top trace: i_{g1} (14 A/div), 2nd trace: i_{g2} (14 A/div), Bottom trace: v_g (200 V/div) and i_g (14 A/div). Time:- (a) 500 ms/div, (b) 20 μs/div, (c) 10 ms/div.

spectively, of the expected values under power balance. This corresponds to Zone A in Fig. 5.10a. A current perturbation of $i_{ptb} = 2$ was injected into the inner fundamental current control loop of DAB1 at $t = t_1$ sec, to determine the values of L_{s1} and L_{s2}. During the addition of i_{ptb}, the overshoot and settling time in v_o were measured to be approximately 3.5 V(1.46%) and 200 ms, respectively. On the DSP control platform, it was observed that the inner H_{iLs} controller generated $d_{\varphi 1nw} = 0.1838$ and $d_{\varphi 2nw} = 0.1356$ for DAB1 and DAB2 respectively. As a result, the $i_{Ls1,rms}$ and $i_{Ls2,rms}$ values were changed to approximately 129.72% and 70.28% respectively, from the anticipated values under power balance. Zone B in Fig. 5.10a, highlights this. Using the expression in (5.24), the HF-link parameters were estimated and the estimation error was found within 4.5%. At $t = t_2$ sec, these estimated values were updated in the state observer blocks. Throughout this transition period, an undershoot of 5 V(2.1%) and a settling time of 250 ms were noted in the load voltage. Eventually, power balance was achieved through the proposed control scheme, corresponding to Zone C. The $i_{Ls1,rms}$ and $i_{Ls2,rms}$ were approximately 103.1% and 96.9% respectively, yielding a current sharing error of 3.1% at the steady state.

Next, the impact of the current perturbation on the input LVDC voltages v_{dc1} and v_{dc2} was examined. The experimental findings are presented in Fig. 5.11. As depicted in Fig. 5.11a, during the transition from Zone A to Zone B the overshoot/undershoot in v_{dc1} and v_{dc2} remains below 8 V(4%) upon the addition of i_{ptb}. The settling time remains below 300 ms. As the system transits from Zone B to Zone C, the overshoot/undershoot stays below 10 V(5%), with a settling time of approximately 320 ms. This is presented in Fig. 5.11b. It is clearly evident from Fig. 5.10 and Fig. 5.11 that, throughout the entire power balance process driven by current perturbation, the DC voltages v_{dc1}, v_{dc2}, and most importantly the load voltage v_o, exhibit smooth and stable operation.

Subsequent experiment was conducted to assess the dynamic behaviour of the proposed control approach during load transients. The experiments outcomes are depicted in Fig.



(a) Zone A to Zone B transition. **(b)** Zone B to Zone C trasition.

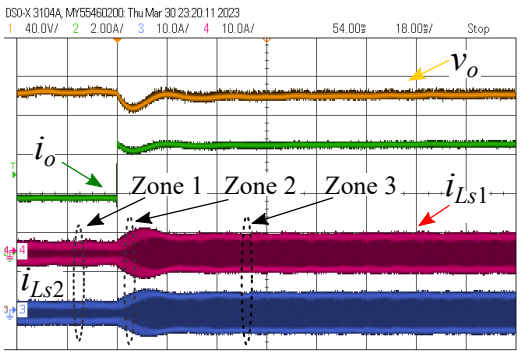
Figure 5.11: Experimental results showing impact of current perturbation and compensation on input LVDC voltages. (a) and (b) Top trace: v_{dc2} (40 V/div), 2nd trace: v_{dc1} (40 V/div), 3rd trace: i_{Ls1} (10 A/div), Bottom trace: i_{Ls2} (10 A/div). Time:- (a) 50 ms/div, (b) 80 ms/div.

5.12. A load current increase of 50% from full load to half load (2.9 A $\rightarrow$ 5.8 A), was given as step load disturbance. The corresponding experimental result is given in Fig. 5.12a. The settling time and undershoot of the load voltage v_o are approximately 15 ms and 5%, respectively. The zoomed views in Zone 1, Zone 2, and Zone 3 depict the current sharing pattern of i_{Ls1} and i_{Ls2} at half load, during transition and at full load respectively, as illustrated in Fig. 5.12b. i_{Ls1} and i_{Ls2} are distributed nearly equally in both steady state and during transients due to the implementation of power balance control. Following this, a step decrease in i_o was initiated from (5.8 A $\rightarrow$ 2.9 A) as depicted in Fig. 5.12c. The settling time and percentage overshoot of v_o are approximately 15 ms and 5%.

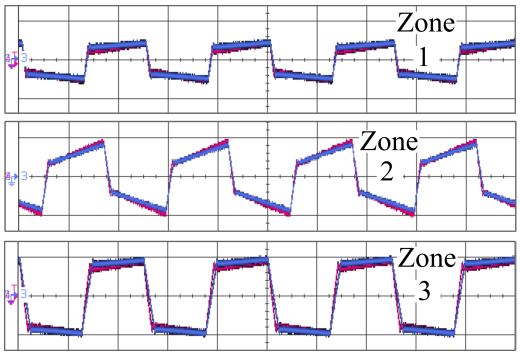
The subsequent experiments were conducted to assess the impact of step load disturbances on the dynamic behaviour of grid-side current and LVDCin voltages. The experimental results are illustrated in Fig. 5.13. In both cases of step load increase and decrease, the settling time of grid current i_g is approximately 60 ms, which is only 3 grid cycles. Throughout these load transients, UPF operation is consistently maintained. Fig. 5.13a and Fig. 5.13b shows the experimental results. The overshoot/undershoot observed in v_{dc1} and v_{dc2} due to the step load disturbance remains below 4% with a settling time of approx-

imately 80 ms. The experimental validation of these findings is shown in Fig. 5.13c and Fig. 5.13d. Additionally, the steady-state IPFEC input currents i_{g1} and i_{g2} at half load are presented in Fig. 5.13e. At half load, the current sharing error was approximately 3.8%. Fig. 5.13f depicts the transition of i_g, i_{g1}, and i_{g2} from half load to full load during the step increase in load. Throughout this transition all these currents remain in the same phase.

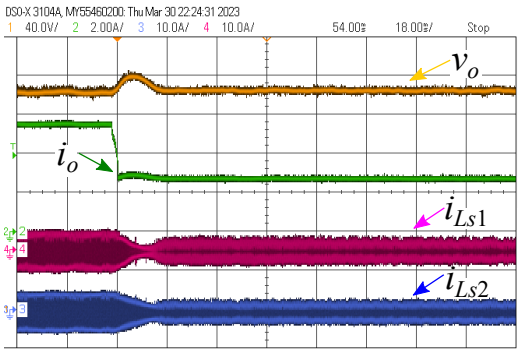
The following experiment was performed to demonstrate the capability of controlled zero power sharing. The current reference for cell2 was suddenly set to zero by changing K_2 to zero. The experimental outcomes are depicted in Fig. 5.14. This experiment was conducted at a load power of 1 kW due to the limitation of having only 2 cells. Upon setting K_2 to zero, entire active power is transferred through cell1, while zero power flows



(a) Step increase in load current.

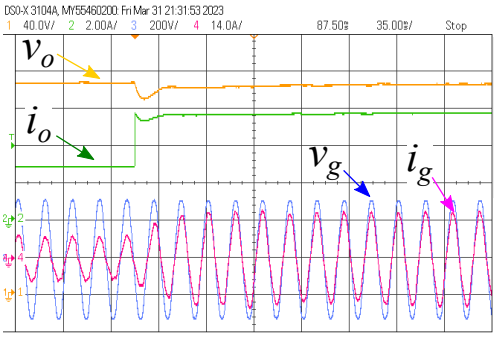


(b) Zoomed view.

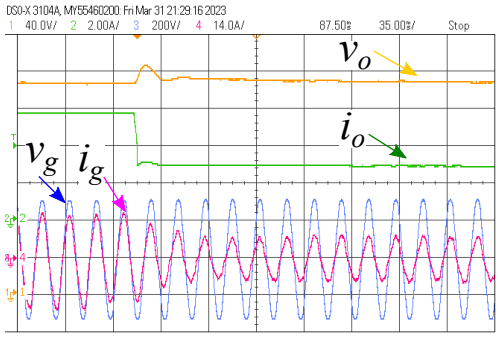


(c) Step decrease in load current.

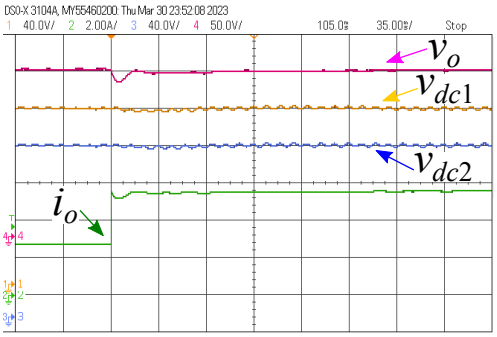
Figure 5.12: Experimental results during load disturbance. (a) & (c) Top trace: v_o (40 V/div), 2nd trace: i_o (2 A/div) , 3rd trace: i_{Ls1} (10 A/div), Bottom trace: i_{Ls2} (10 A/div). (b) Upper trace: Zone 1, Middle trace: Zone 2, Bottom trace: Zone 3. Time:- (a) & (c) 18 ms/div, (b) 20 μs/div.



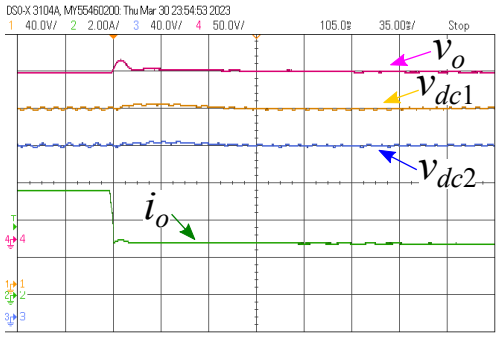
(a) v_g and i_g during load increase.



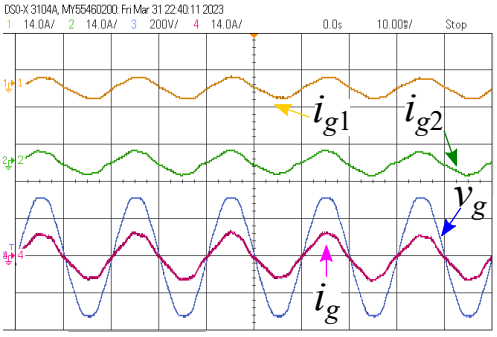
(b) v_g and i_g during load decrease.



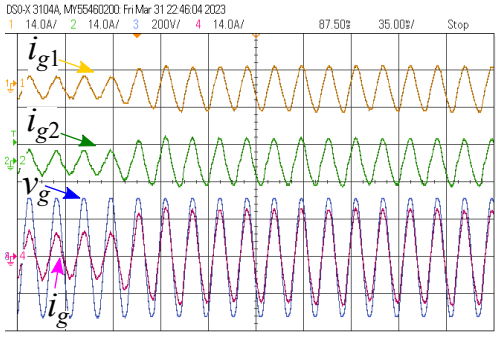
(c) LVDCins during load increase.



(d) LVDCins during load decrease.



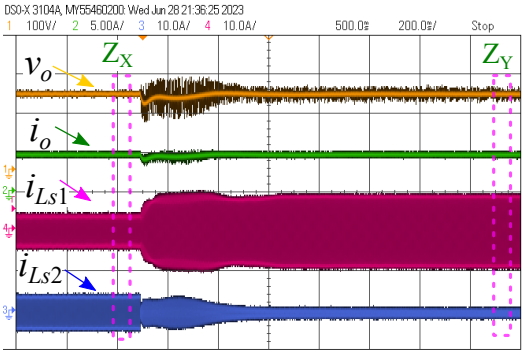
(e) Half load operation.



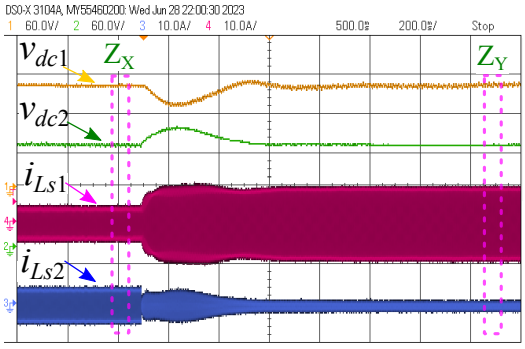
(f) Grid side currents.

Figure 5.13: Experimental results showing v_g, i_g, i_{g1}, i_{g2}, v_{dc1} and v_{dc2} during 50% step load transient. (a) and (b) Top trace: v_o (40 V/div), 2nd trace: i_o (2 A/div), 3rd trace: v_g (200 V/div), Bottom trace: i_g (14 A/div). (c) and (d) Top trace: v_o (50 V/div), 2nd trace: v_{dc1} (40 V/div), 3rd trace: v_{dc2} (40 V/div), Bottom trace: i_o (2 A/div). (e) and (f) Top trace: i_{g1} (14 A/div), 2nd trace: i_{g2} (14 A/div), Bottom trace: v_g (200 V/div) and i_g (14 A/div). Time:- (a), (b), (c), (d), (f) 35 ms/div. (e) 10 ms/div.

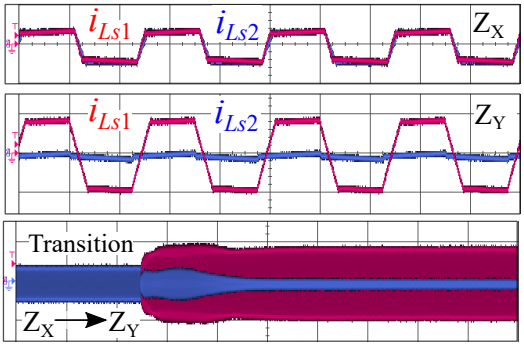
through cell2 in the steady state, as shown in Fig. 5.14a. Additionally, input voltages v_{dc1} and v_{dc2} are equally regulated at 165 V, as given in Fig. 5.14b. i_{Ls1} and i_{Ls2} are equal in the equal power sharing mode, corresponding to Zone X (Zx). When K_2 is set to zero,



(a) v_o and i_o during 2^{nd} cell shutdown.



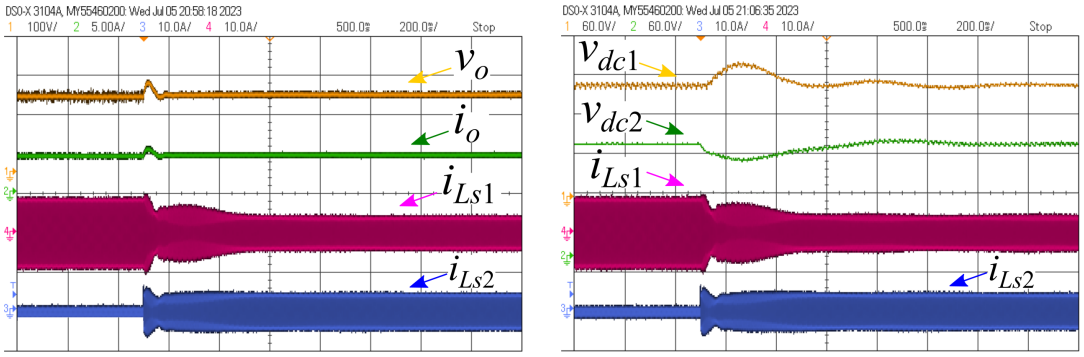
(b) LVDC input voltages during 2^{nd} cell shutdown.



(c) i_{Ls1}, i_{Ls2}: zoomed view and their transition.

Figure 5.14: Experimental results showing controlled zero power sharing (phase shedding) for cell 2. (a) Top trace: v_o (100 V/div), 2nd trace: i_o (5 A/div) , 3rd trace: i_{Ls1} (10 A/div), Bottom trace: i_{Ls2} (10 A/div). (b) Top trace: v_{dc1} (60 V/div), 2nd trace: v_{dc2} (60 V/div) , 3rd trace: i_{Ls1} (10 A/div), Bottom trace: i_{Ls2} (10 A/div). (c) Zoomed view of superimposed i_{Ls1} and i_{Ls2} (10 A/div). Time:- (a) & (b) 200 ms/div, (c) 20 μs/div.

the power in cell2 becomes zero. This results in doubling of i_{Ls1} and i_{Ls2} reaches almost zero. This corresponds to Zone y(Zy), as illustrated in Fig. 5.14c. The i_{Ls2} waveform still contains very small switching ripple and second harmonic ripple current. During periods of low load demand, this zero power sharing feature can facilitate controlled shutdowns of cells, enabling other cells to operate closer to their rated conditions. Throughout this lean period, the LVDCin voltages in the deactivated cells remain regulated. Therefore during load increments, these cells can be swiftly reactivated to contribute to power delivery since their capacitors are already charged. The process of adding cell2 back into operation is illustrated in Fig. 5.15. Throughout this transition the settling time of v_o is approximately



(a) v_o and i_o during plug-in. **(b)** LVDCin voltages during plug-in.

Figure 5.15: Experimental results showing controlled phase addition of cell2. (a) Top trace: v_o (100 V/div), 2nd trace: i_o (5 A/div). (b) Top trace: v_{dc1} (60 V/div), 2nd trace: v_{dc2} (60 V/div). 3rd trace of (a) & (b): i_{Ls1} (10 A/div), Bottom trace of (a) & (b): i_{Ls2} (10 A/div). Time:- (a) and (b) 200 ms/div.

70 ms, as depicted in Fig. 5.15a. Given that the capacitors are precharged, there is no need for an additional precharge circuit in the proposed control scheme.

A simulation was conducted for a three-cell configuration to verify the control strategy using PLECS. The simulation results are shown in Fig. 5.16. The HF-link inductance values for the three cells are set as follows: $L_{s1} = 210\mu$H, $L_{s2} = 250\mu$H, and $L_{s3} = 290\mu$H. The rated output voltage (v_o) and total load power are 400 V and 3600 W respectively. Prior to $t = t_1$, all three DABs operate in common phase-shift duty (CPSD) mode with ($d_{\varphi 1} = d_{\varphi 2} = d_{\varphi 3} = d_{\varphi c}$). At $t = t_1$, perturbation is introduced in DAB1 by locking the phase-shift of DAB3 ($d_{\varphi 3} = d_{\varphi c}$). The phase-shift duty ratio of DAB1 and DAB2 in this FCP stage resulted in λ_2/λ_1 calculated as 1.185. At $t = t_2$, CPSD mode was reinstated by removing the perturbation from DAB1. Following this, at $t = t_3$, phase-shift duty of DAB2 was fixed as ($d_{\varphi 2} = d_{\varphi c}$) and a perturbation was introduced in DAB1. In a similar manner, based on the phase-shift duty ratios of DAB1 and DAB3, λ_3/λ_1 was computed as 1.372. Eventually, power balance was attained after t_4 with a current sharing error of approximately 1.5% in the steady state. Throughout this process, the overshoot/undershoot in v_o remained below $\pm 1.5\%$.

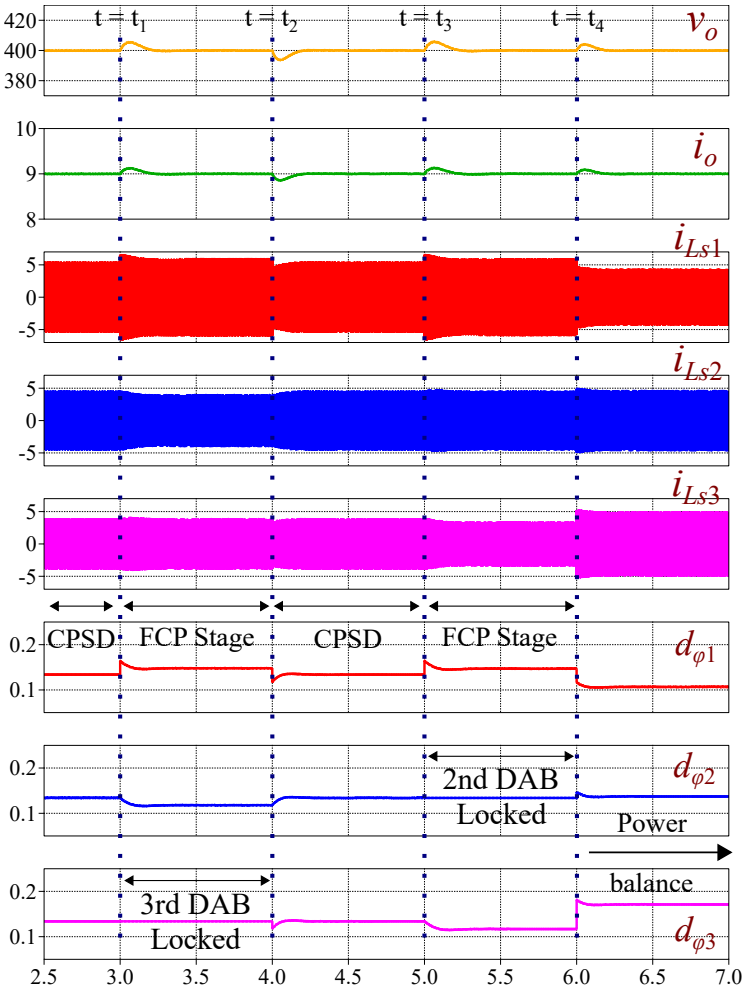


Figure 5.16: Simulation waveforms for three cell.

5.5.1 Communication and Synchronization in Modular SSTs

Modular SSTs can be connected in parallel or series configurations. The modular design inherently supports scalability in voltage and power levels by adding or removing converter cells. While large-scale modular systems introduce challenges related to communication and synchronization, these can be effectively addressed using CAN or Ethernet-based communication protocols. For instance, considering a sampling rate of 20 kHz and a 12-bit ADC resolution, the data rate per variable is:

$$20000 \times 12 = 240 \text{ kbps} = 0.24 \text{ Mbps}.$$

In one SST cell, there are control variables including FEC output voltage v_{dc1}, i_{Ls1}, d_{φ_1}, d_{d1}, and d_{q1}, approximately 5 in total. Additionally, v_g, i_{gd}, i_{gq}, v_o, and i_o are common for all cells. Assuming there are 10 cells, the total number of variables is nearly 55. The total required bandwidth is:

$$55 \times 0.24 = 13.2 \text{ Mbps}.$$

Given that CAN FD supports 5–8 Mbps, it may not be sufficient for large-scale systems. In contrast, Fast Ethernet, EtherCAT, or TSN-based Real-Time Ethernet (100 Mbps – 1 Gbps) can handle higher data rates efficiently. Synchronization between cells can be ensured using phase-locked loops (PLLs) or centralized master-slave coordination. However, if the communication bandwidth requirement is lower, CAN FD remains a cost-effective option.

5.6 Concluding Remarks

A flexible power sharing control strategy for IPOP AC-DC converter is detailed in this chapter. This approach achieves unity power factor (UPF) operation and voltage balance using only one current sensor on the grid side, by adjusting the reactive component of FEC duty cycles to accommodate variations in grid interfacing inductance and HF-link inductance. Central to the control strategy is the utilization of the HF-link current fundamental harmonic active component as a crucial control variable for flexible power transfer. This allows for both equal and zero power sharing. An online estimation method for HF-link parameters and its fundamental current, inspired by a perturbation algorithm is also discussed in this chapter. Notably this approach requires only load current and grid current measurements. It eliminates the requirement of any HBW current sensor or each cell-to-cell current measurement. All the aforementioned features of the proposed control scheme have been validated through experiments.

Chapter 6

Conclusion

This thesis has attempted to devise high frequency current sensorless control strategies for single cell dual active bridge (DAB) converters, input-series-output-parallel (ISOP) modular SSTs and input-parallel-output-parallel (IPOP) AC-DC systems. The conclusions of the study and key contributions of this research work are provided here.

6.1 Conclusions and Contribution

The conclusions and contributions are outlined as follows,

Modelling:

The presented analysis began with the conventional small signal analysis of CMFEC plant model in synchronous dq reference frame and small signal analysis of modular DAB using Generalised average (GA) model. The relevant transfer functions are derived from the small signal model, which provides the system designer more meaningful insights for design considerations. The effect of equal/unequal modulation duty cycles of FECs on the quality of current drawn from grid is analysed. Unlike the reduced-order model, the GA model effectively captures the dynamics of HF-link current, as validated by relevant simulations.

HF-Link Current Estimation:

A dual-loop control strategy for a single cell DAB is presented using HF-link current fundamental and peak envelope estimation. It addresses the constraints associated with the use of HBW current sensors. Therefore, the necessity for HBW current sensors is eliminated, relying instead on estimated inductor current for feedback. Experimentally it has been demonstrated that estimating the envelope instead of the total current is equally effective for overcurrent limitation, offering a solution with low computation and cost-effectiveness.

Flexible Power Sharing Control for Modular ISOP SST:

A HBW current sensorless flexible power sharing control strategy for modular ISOP SST is presented by controlling the active component of HF-Link current fundamental envelope. This addresses the loss of an entire degree of freedom in the topology and its inability to perform flexible power sharing due to the fixed/common modulation duty cycle in all FECs of CMFEC. Therefore, a flexible power sharing control strategy is formulated while still regulating the MVDC voltages without requiring additional precharge circuits. Experimentally it has been validated that despite parametric variations in the HF-link of SST cells, the current sharing error remains minimal across a wide range of load power.

Flexible Power Sharing Control for IPOP AC-DC Converter:

A flexible power sharing control strategy for IPOP AC-DC converters has been detailed. Utilizing only one current sensor on the grid side, the strategy achieves UPF operation of all parallel units and voltage balance of all intermediate DC link capacitors by adjusting the reactive component of FEC modulation duty cycles. An online estimation technique for HF-link parameter inspired by a fundamental current perturbation algorithm is devised to enhance the robustness of the flexible power sharing control approach. These features have been extensively validated through experiments.

6.2 Future Work

Future research could explore several innovative concepts at both the architectural and control levels. These are outlines as follows:

- Adopting a 3-phase modular multilevel front-end converter instead of a 1-phase configuration can improve the power density of the entire system by bringing down the size of MVDC capacitors, due to the absence of second harmonic power in 3-phase AC-DC systems.

- Low-voltage lithium-ion batteries (48V) are currently the preferred choice for home energy storage applications. They offer high energy density, greater cost-effectiveness and longer lifetimes. Additionally, they reduce compliance requirements as they fall under the safety extra-low voltage (SELV) system. Integrating a 48V battery with the grid requires bidirectional DC-DC boosting/bucking conversion (Most preferably DAB DC-DC topology) by approximately ten times, as the grid-side DC-link voltage is typically 400V. In 1-phase residential applications, the inverter is also 1-phase, which generates second harmonic ripple at the 400V DC-link. If this ripple is absorbed entirely by the DC-link capacitor, it requires bulky capacitors reducing power density. Conversely, diverting the second harmonic ripple to the 48V battery side, where it is boosted nearly ten times, can drastically reduce the lifespan of battery. Therefore, this second harmonic current can be controlled and split between capacitor and battery to optimize the size of the DC-link capacitor and extend the lifetime of battery, while still meeting the targeted mission profile. The second harmonic ripple current, superimposed on the average fundamental current, amplifies the peak-to-peak current ripple. It would be interesting to investigate, its effect on the size of HF-link magnetics and their saturation boundaries.

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List of Publications

Journals

1. G. Nayak and A. Dasgupta, "Inductor Current Envelope Tracking-Based Sensorless Control of Dual Active Bridge Converter," in IEEE Transactions on Power Electronics, vol. 37, no. 7, pp. 7907-7915, July 2022, doi: 10.1109/TPEL.2022.3151503.

2. G. Nayak and A. Dasgupta, "Control of Utility Interfacing Modular High Frequency AC Link Converter Based on Fundamental Current Estimation," in IEEE Access, vol. 12, pp. 38867-38884, 2024, doi: 10.1109/ACCESS.2024.3376386.

3. G. Nayak and A. Dasgupta, "Flexible Power Sharing Control of Isolated Input-Parallel-Output-Parallel AC-DC Converters Based on High Frequency Link Current Estimation," in IEEE Transactions on Industry Applications, vol. 61, no. 1, pp. 1268-1279, Jan.-Feb. 2025, doi: 10.1109/TIA.2024.3477474.

Conferences

1. G. Nayak and A. Dasgupta, "Full Order Averaged Modelling for Modular Solid State Transformer," 2020 IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES), Jaipur, India, 2020, pp. 1-6, doi: 10.1109/PEDES 49360.2020.9379573.

2. G. Nayak and A. Dasgupta, "Observer Based Current Control of Dual Active Bridge

Converter," 2022 IEEE International Conference on Power Electronics, Smart Grid, and Renewable Energy (PESGRE), Trivandrum, India, 2022, pp. 1-6, doi: 10.1109/PESGRE52268.2022.9715803.

3. G. Nayak and A. Dasgupta, "Series Inductance Estimation of Dual Active Bridge Converter in Solid State Transformer," 2022 IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES), Jaipur, India, 2022, pp. 1-5, doi: 10.1109/PEDES56012.2022.10080504.

4. G. Nayak and A. Dasgupta, "Flexible Power Sharing Control of Modular Isolated Input-Parallel-Output-Parallel AC-DC Converters Based on High Frequency Link Current Estimation," 2023 IEEE International Conference on Power Electronics, Smart Grid, and Renewable Energy (PESGRE), Trivandrum, India, 2023, pp. 1-6, doi: 10.1109/PESGRE58662.2023.10405309.

5. Y. S. Yadav, G. Nayak and A. Dasgupta, "A Generic Current Sensorless Control Scheme for Dual Active Bridge Converter," 2022 IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES), Jaipur, India, 2022, pp. 1-6, doi: 10.1109/PEDES56012.2022.10080530.

Appendix A

Theorems Associated with Properties of Complex Fourier Series

Theorem A.1 (Time differential property of FS)**.**

$$\textit{if,} \quad x(\tau) \xrightarrow{k^{th}FC} \langle x \rangle_k(t), \tag{A.1}$$

then,

$$\frac{dx(\tau)}{dt} \xrightarrow{k^{th}FC} \left\{ \frac{d}{dt} \langle x \rangle_k(t) \right\} + jk\omega \langle x \rangle_k(t). \tag{A.2}$$

Proof :

$$\begin{aligned} x(\tau) &= \sum_{k=-\infty}^{\infty} \langle x \rangle_k(t) e^{jk\omega\tau} \\ \frac{dx(\tau)}{dt} &= \sum_{k=-\infty}^{\infty} \frac{d}{dt} \Big[\langle x \rangle_k(t) e^{jk\omega\tau} \Big] = \sum_{k=-\infty}^{\infty} \Big[\Big\{ \frac{d}{dt} \langle x \rangle_k(t) \Big\} + jk\omega \langle x \rangle_k(t) \Big] e^{jk\omega\tau} \end{aligned} \tag{A.3}$$

k^{th} Fourier coefficient (FC) of $\dfrac{dx(\tau)}{dt}$ is denoted by $\left\langle \dfrac{dx(\tau)}{dt} \right\rangle_k (t)$.

$$\begin{aligned} \left\langle \frac{dx(\tau)}{dt} \right\rangle_k (t) &= \frac{d}{dt}\langle x \rangle_k(t) + jk\omega\langle x \rangle_k(t) \\ \frac{d}{dt}\langle x \rangle_k(t) &= \left\langle \frac{dx(\tau)}{dt} \right\rangle_k (t) - jk\omega\langle x \rangle_k(t) \\ \frac{dx(\tau)}{dt} &\xrightarrow{k^{th}FC} \left\{ \frac{d}{dt}\langle x \rangle_k(t) \right\} + jk\omega\langle x \rangle_k(t) \end{aligned} \tag{A.4}$$

Theorem A.2 (Modulation or Multiplication Property of Fourier Series)**.**

$$\textit{if,} \quad x(\tau) \xrightarrow{k^{th}FC} \langle x \rangle_k \qquad \textit{and} \qquad y(\tau) \xrightarrow{k^{th}FC} \langle y \rangle_k \tag{A.5}$$

then,

$$x(\tau)y(\tau) \xrightarrow{k^{th}FC} \sum_{i=-\infty}^{\infty} \langle x(\tau) \rangle_{k-i} \langle y(\tau) \rangle_i \tag{A.6}$$

Proof :

$$\begin{aligned} \langle x(\tau)y(\tau) \rangle_k &= \frac{1}{T}\int_{\tau=(t-T)}^{t} \Big[x(\tau)y(\tau) \Big] e^{-jk\omega\tau} d\tau \\ &= \frac{1}{T}\int_{\tau=(t-T)}^{t} \Big[x(\tau) \sum_{i=-\infty}^{\infty} \langle y(\tau) \rangle_i e^{ji\omega\tau} \Big] e^{-jk\omega\tau} d\tau \\ &= \sum_{i=-\infty}^{\infty} \frac{1}{T}\int_{\tau=(t-T)}^{t} \Big[x(\tau) e^{-j(k-i)\omega\tau} d\tau \Big] \langle y(\tau) \rangle_i = \sum_{i=-\infty}^{\infty} \langle x(\tau) \rangle_{k-i} \langle y(\tau) \rangle_i \end{aligned} \tag{A.7}$$

Appendix B

Derivation of EFHA Model

B.0.1 Modification of the state variables

After calculation of ε, it can be taken in to account for all state variables to get a more accurate dynamic model. In this EFHA model all the state variables are modified. The state variables of previously discussed FHA based GA model were $\langle v_o \rangle_0$, $\langle i_{Ls} \rangle_1^I$ and $\langle i_{Ls} \rangle_1^R$. The newly modified state variables of EFHA based GA model are denoted as $\langle v_{om} \rangle_0$, $\langle i_{Lsm} \rangle_1^I$ and $\langle i_{Lsm} \rangle_1^R$. These modified state variables are derived subsequently.

Modification of $\langle v_o \rangle_0$ state variable

Without the inclusion of modification factor, the active power transfer due to only fundamental component is given in (3.21). Modified $\langle v_{om} \rangle_0$ is substituted in (3.21) in place of $\langle v_o \rangle_0$ to obtain modified fundamental active power (p_{fundm}) as,

$$p_{fundm} = \frac{8}{\pi^2} \frac{N_t \langle v_{dc} \rangle_0 \langle v_{om} \rangle_0}{\omega L_s} \sin\varphi = p_{DAB}. \tag{B.1}$$

This modification is done to match p_{fundm} equal to p_{DAB}, which is given by,

$$p_{DAB} = p_{fundm} = \varepsilon \, p_{fund} = \varepsilon \frac{8}{\pi^2} \frac{N_t \langle v_{dc} \rangle_0 \langle v_o \rangle_0}{\omega L_s} \sin\varphi. \tag{B.2}$$

Solving (B.1) and (B.2), the expression for $\langle v_{om} \rangle_0$ can be obtained as,

$$\langle v_{om} \rangle_0 = \varepsilon \, \langle v_o \rangle_0. \tag{B.3}$$

Modification of $\langle i_{Ls} \rangle_1^R$ state variable

The reactive power transfer due to fundamental component without including the modification factor is given in (3.22). $\langle v_{om} \rangle_0$ is substituted in place of $\langle v_o \rangle_0$ to obtain modified fundamental reactive power (q_{fundm}) as,

$$q_{fundm} = \frac{8}{\pi^2} \frac{\langle v_{dc} \rangle_0}{\omega L_s} \big[\langle v_{dc} \rangle_0 - N_t \langle v_{om} \rangle_0 \cos \varphi \big]. \tag{B.4}$$

After substituting (B.3) in (B.4) and then solving (3.22) and (B.4), the relationship between q_{fundm} and q_{fund} can be derived as,

$$q_{fundm} = \varepsilon \, q_{fund} - (\varepsilon - 1) \frac{8}{\pi^2} \frac{\langle v_{dc} \rangle_0^{\,2}}{\omega L_s}. \tag{B.5}$$

Using the equations (2.28), (2.30), (2.48), (2.49) and applying fundamental harmonic approximation the p_{fund} and q_{fund} can also be derived as,

$$p_{fund} \;=\; 2\big[\langle v_{pri} \rangle_1^R \langle i_{Ls} \rangle_1^R + \langle v_{pri} \rangle_1^I \langle i_{Ls} \rangle_1^I \big] = -\frac{4}{\pi} \langle v_{dc} \rangle_0 \langle i_{Ls} \rangle_1^I, \tag{B.6}$$

$$q_{fund} \;=\; 2\big[-\langle v_{pri} \rangle_1^R \langle i_{Ls} \rangle_1^I + \langle v_{pri} \rangle_1^I \langle i_{Ls} \rangle_1^R \big] = -\frac{4}{\pi} \langle v_{dc} \rangle_0 \langle i_{Ls} \rangle_1^R. \tag{B.7}$$

The above expression shows that $\langle i_{Ls} \rangle_1^I$ is the active power component and $\langle i_{Ls} \rangle_1^R$ is the reactive power component of the inductor current. Modified $\langle i_{Lsm} \rangle_1^R$ is substituted in place of $\langle i_{Ls} \rangle_1^R$ in (B.7) to arrive at,

$$q_{fundm} = -\frac{4}{\pi}\langle v_{dc}\rangle_0 \langle i_{Lsm}\rangle_1^R \tag{B.8}$$

Solving (B.5), (B.7) and (B.8), relation between $\langle i_{Ls}\rangle_1^R$ and $\langle i_{Lsm}\rangle_1^R$ can be derived as,

$$\langle i_{Lsm}\rangle_1^R = \varepsilon \langle i_{Ls}\rangle_1^R + (\varepsilon - 1)\frac{2}{\pi}\frac{\langle v_{dc}\rangle_0}{\omega L_s} \tag{B.9}$$

Modification of $\langle i_{Ls}\rangle_1^I$ state variable

Modified $\langle i_{Lsm}\rangle_1^I$ can be substituted in place of $\langle i_{Ls}\rangle_1^I$ in (B.6) to arrive at,

$$p_{fundm} = -\frac{4}{\pi}\langle v_{dc}\rangle_0 \langle i_{Lsm}\rangle_1^I. \tag{B.10}$$

Substituting (B.6) and (B.10) in (B.2), relationship between $\langle i_{Ls}\rangle_1^I$ and $\langle i_{Lsm}\rangle_1^I$ can be obtained as,

$$\langle i_{Lsm}\rangle_1^I = \varepsilon \langle i_{Ls}\rangle_1^I. \tag{B.11}$$

EFHA based GA Large signal model

Modified state variables in (B.3), (B.9) and (B.11) are substituted in the earlier derived state space dynamic model to derive EFHA based large signal model, which is given by,

EFHA based GA small signal model

Linearisation of the EFHA based large signal model is done by adding small perturbation to the control input. The simplified linearised terms used during derivation of modified small signal model are,

$$\frac{1}{\varepsilon} \xrightarrow{\text{Linearised}} \frac{1}{E}\big(1 + K_x\hat{d}_\varphi\big), \tag{B.13}$$

$$\varepsilon \xrightarrow{\text{Linearised}} E\big(1 - K_x\hat{d}_\varphi\big), \tag{B.14}$$

$$\begin{bmatrix} \langle \dot{v}_{om} \rangle_0 \\ \langle \dot{i}_{Lsm} \rangle_1^R \\ \langle \dot{i}_{Lsm} \rangle_1^I \end{bmatrix} = \begin{bmatrix} -\dfrac{1}{\varepsilon R_o C_o} & -\dfrac{4N_t \sin(\pi d_\varphi)}{\pi C_o} & -\dfrac{4N_t \cos(\pi d_\varphi)}{\pi C_o} \\ \dfrac{2N_t \sin(\pi d_\varphi)}{\pi L_s} & -\dfrac{R_s}{L_s} & \omega \\ \dfrac{2N_t \cos(\pi d_\varphi)}{\pi L_s} & -\omega & -\dfrac{R_s}{L_s} \end{bmatrix} \begin{bmatrix} \langle v_{om} \rangle_0 \\ \langle i_{Lsm} \rangle_1^R \\ \langle i_{Lsm} \rangle_1^I \end{bmatrix} + \begin{bmatrix} 0 \\ \dfrac{2(\varepsilon - 1)}{\pi \omega L_s} \left\{ \dfrac{R_s}{L_s} + \dfrac{d}{dt} \right\} \\ -\dfrac{2}{\pi L_s} \end{bmatrix} v_{dc} + \begin{bmatrix} -\dfrac{1}{\varepsilon C_o} \\ 0 \\ 0 \end{bmatrix} i_N. \tag{B.12}$$

$$\sin[\pi(\hat{d}_\varphi + D_\varphi)] \xrightarrow{\text{Linearised}} \sin(\pi D_\varphi) + \pi \hat{d}_\varphi \cos(\pi D_\varphi), \tag{B.15}$$

$$\cos[\pi(\hat{d}_\varphi + D_\varphi)] \xrightarrow{\text{Linearised}} \cos(\pi D_\varphi) - \pi \hat{d}_\varphi \sin(\pi D_\varphi), \tag{B.16}$$

where,

$$E = \frac{\pi^3}{8} \frac{D_\varphi (1 - D_\varphi)}{\sin(\pi D_\varphi)}, \tag{B.17}$$

$$K_x = \pi \cot(\pi D_\varphi) - \frac{(1 - 2D_\varphi)}{D_\varphi (1 - D_\varphi)}. \tag{B.18}$$

After linearisation, the linearised EFHA modified small signal model is derived as,

$$\begin{bmatrix} \langle \hat{\dot{v}}_{om} \rangle_0 \\ \langle \hat{\dot{i}}_{Lsm} \rangle_1^R \\ \langle \hat{\dot{i}}_{Lsm} \rangle_1^I \end{bmatrix} = \begin{bmatrix} -\dfrac{1}{E R_o C_o} & -\dfrac{4N_{sin}}{\pi C_o} & -\dfrac{4N_{cos}}{\pi C_o} \\ \dfrac{2N_{sin}}{\pi L_s} & -\dfrac{R_s}{L_s} & \omega \\ \dfrac{2N_{cos}}{\pi L_s} & -\omega & -\dfrac{R_s}{L_s} \end{bmatrix} \begin{bmatrix} \langle \hat{v}_{om} \rangle_0 \\ \langle \hat{i}_{Lsm} \rangle_1^R \\ \langle \hat{i}_{Lsm} \rangle_1^I \end{bmatrix} + \begin{bmatrix} 0 \\ \dfrac{2(E-1)}{\pi \omega L_s} \left\{ \dfrac{R_s}{L_s} + \dfrac{d}{dt} \right\} \\ -\dfrac{2}{\pi L_s} \end{bmatrix} \hat{v}_{dc}$$
$$+ \begin{bmatrix} \dfrac{4}{C_o} \left\{ N_{sin} I_{Ls1Im} - N_{cos} I_{Ls1Rm} \right\} - \left\{ \dfrac{V_{om}}{R_o} + i_N \right\} \dfrac{K_x}{E C_o} \\ \dfrac{2N_{cos}}{L_s} V_{om} - \dfrac{2}{\pi \omega L_s} E V_{dc} K_x \left\{ \dfrac{R_s}{L_s} + \dfrac{d}{dt} \right\} \\ -\dfrac{2N_{sin}}{L_s} V_{om} \end{bmatrix} \hat{d}_\varphi + \begin{bmatrix} -\dfrac{1}{E C_o} \\ 0 \\ 0 \end{bmatrix} \hat{i}_N \tag{B.19}$$